

Compal Confidential

Schematics Document

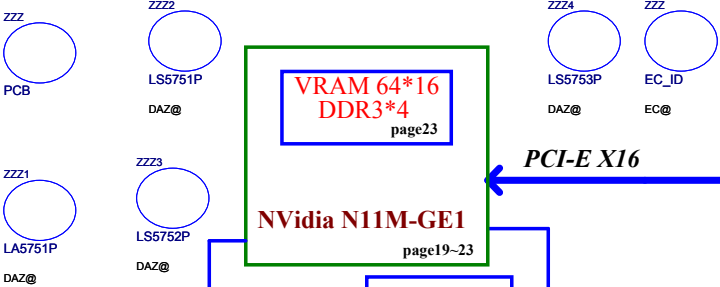
NIWE1

Arrandale

with Intel IBEX PEAK-M core logic

REV: 1.0

Security Classification	Compal Secret Data			Compal Electronics, Ltd.		
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Cover Sheet	
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DDR3 Voltage Rails

power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
				State
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW									
SMB_EC_CK2	KB926	X	X	X	X	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW											+3VALW
SMBCLK	PCH	V	X	X	V	V	X	X	X	X	V	X
SMBDATA	+3VALW	+3VALW			+3VS	+3VS					+3VS	
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW											
SML1CLK	PCH	X	X	V	X	X	X	V	X	V	X	X
SML1DATA	+3VALW			+3VALW				+3VS		+3VS		

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

@ FUNCTION

Structure	Description	NON-USE
45@	45 BOM	
BT@	Blue Tooth function	
3G@	3G function (WWAN)	
CMOS@	CMOS CAMERA function	
ESATA@	E-SATA function	
HDMI@	HDMI function (UMA or DIS)	
UMA HDMI@	HDMI function (UMA only)	
X76@	X76 BOM	
100@	10/100 LAN function	
GIGA@	GIGA LAN function	
UMA@	UMA only (Arrandale)	
DIS@	DIS only (Arrandale)	

SKU

Arrandale (dGPU) DIS only	DIS@
Arrandale (iGPU) UMA only	UMA@

PCIE PORT LIST

PORT	DEVICE
1	
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	
7	
8	

USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
1	LEFT SIDE
2	CMOS
3	RIGHT SIDE
4	
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

VGA and DDR3 Voltage Rails (N11x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	N/A	
GPIO8	I/O	N/A	
GPIO9	OUT	N/A	
GPIO10	OUT	N/A	
GPIO11	I/O	-	Reserve 10K pull low.
GPIO12	IN	N/A	
GPIO13	OUT	N/A	
GPIO14	OUT	-	Reserve 10K pull low.
GPIO15	IN	N/A	
GPIO16	OUT	N/A	
GPIO17	IN	-	PAD
GPIO18	IN	N/A	
GPIO19	IN	N/A	

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

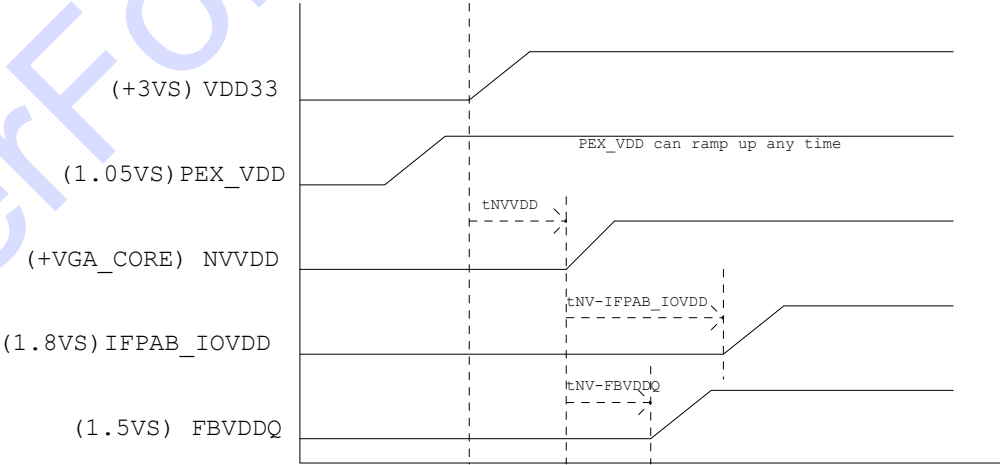
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N11M-GE1 64bit 512MB DDR3	14.02	2.16	TBD	TBD	12.9	12.26	0.66	0.99	1.3	1.95	530	0.56	84	0.15	140	0.15	38	0.13

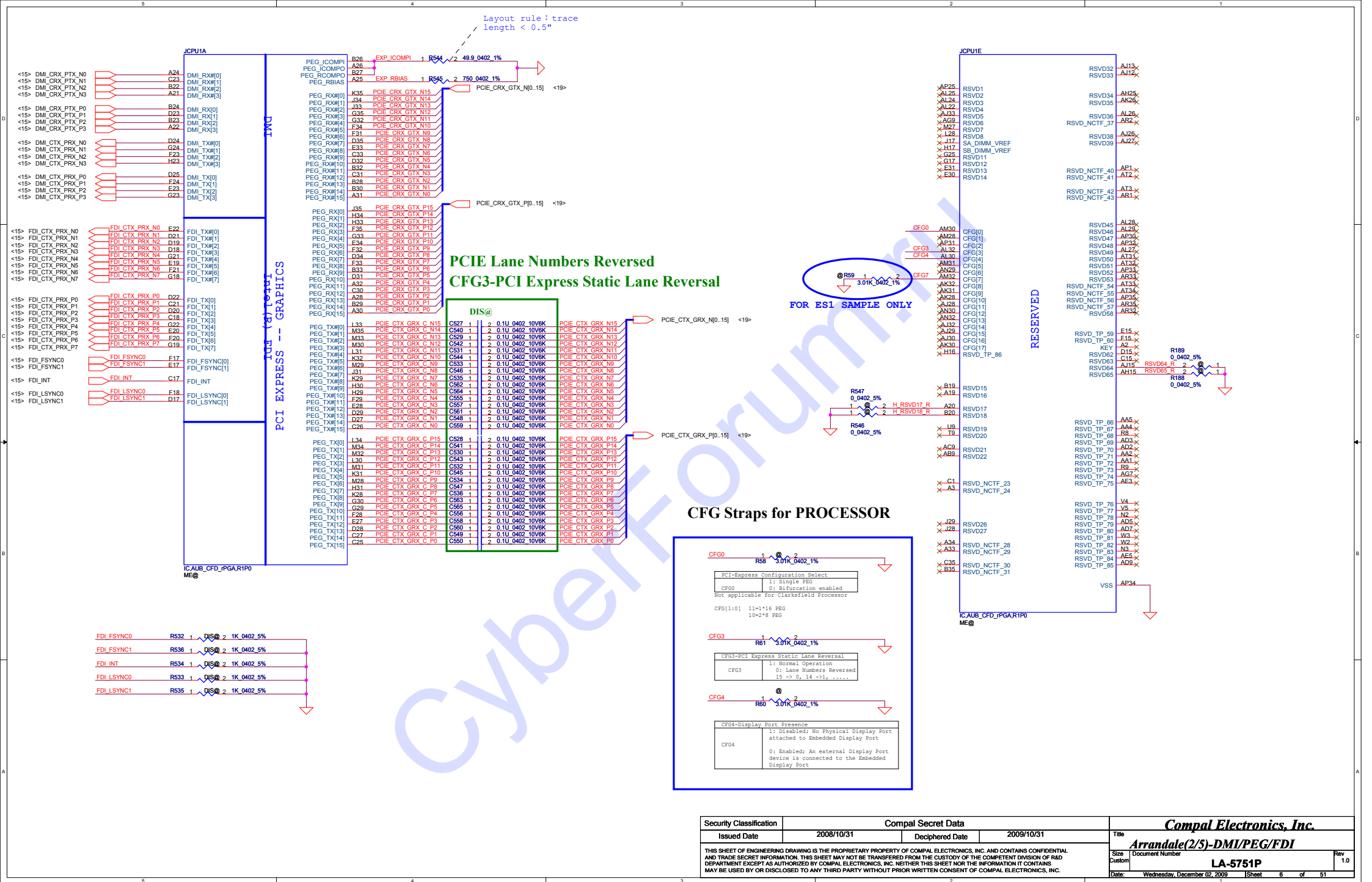
GPIO5 GPIO6

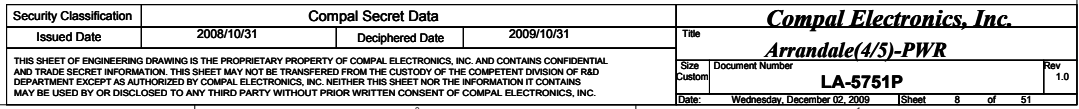
	Device ID	GPU_VID0	GPU_VID1	VGA_CORE	P-State
N11M-GE1/LP1 (40nm)	0x0A7D	0	0	0.8V	Deep P12
		0	1	0.85V	P8
		1	1	1.03V	P0

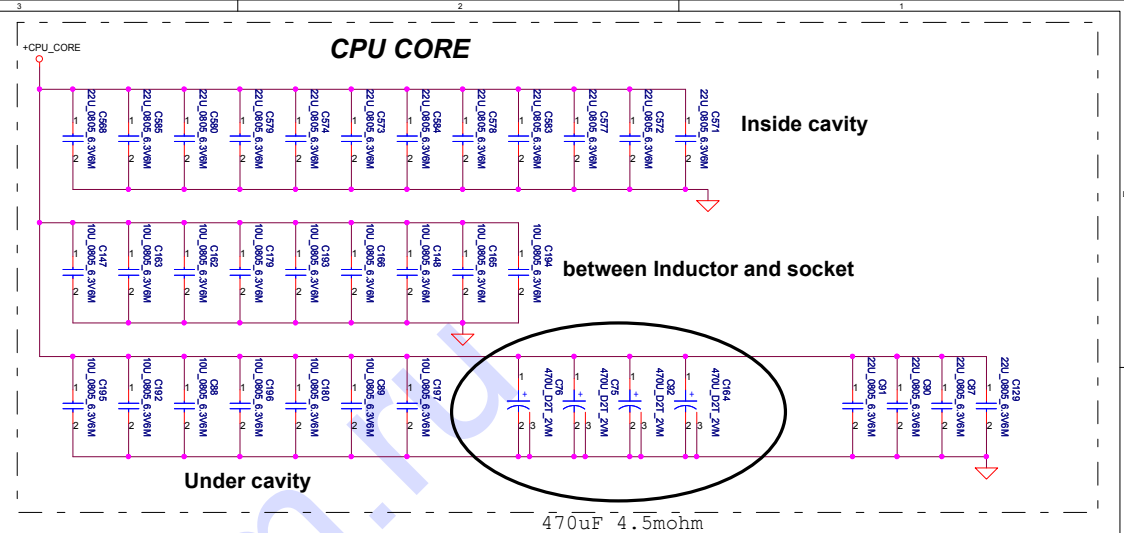
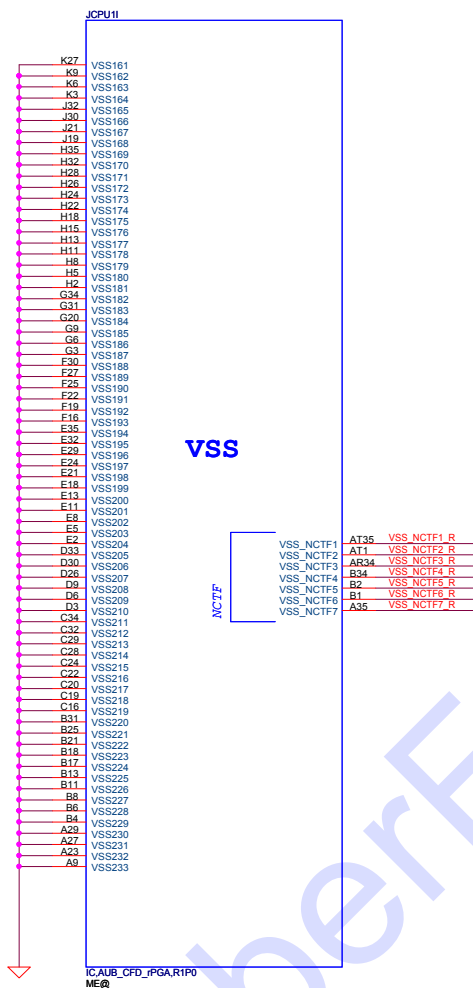
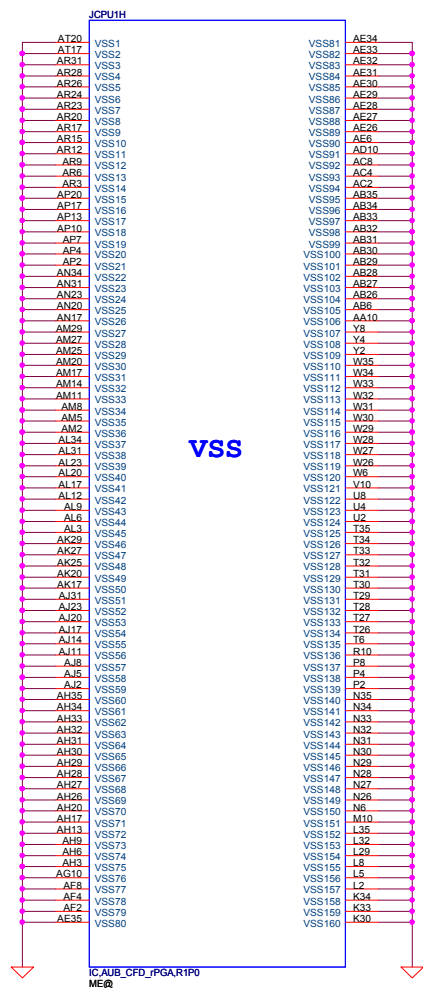
Power Sequence

The ramp time for any rail must be more than 40us

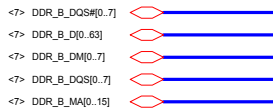




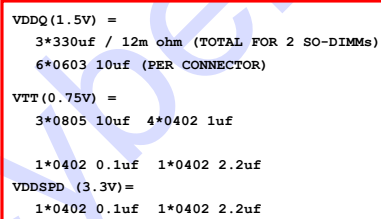
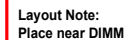




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Layout Note:
Place near DIMM

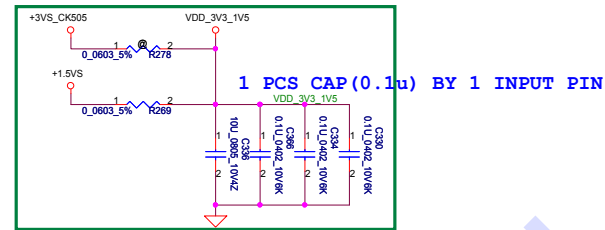


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Reserve for Low Power CLK GEN.

RTM890N-631 (SA00003HQ10)

SLG8LV597VTR (SA00003MF00)



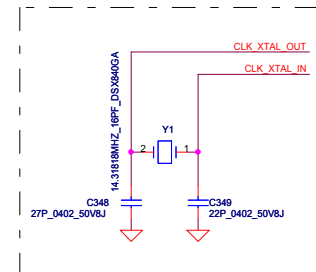
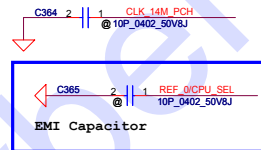
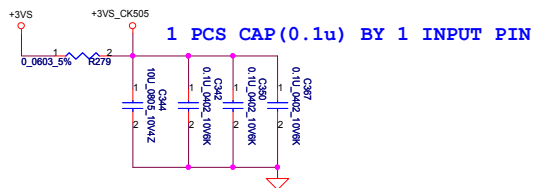
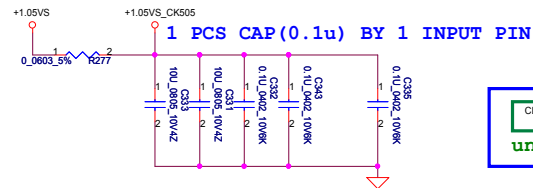
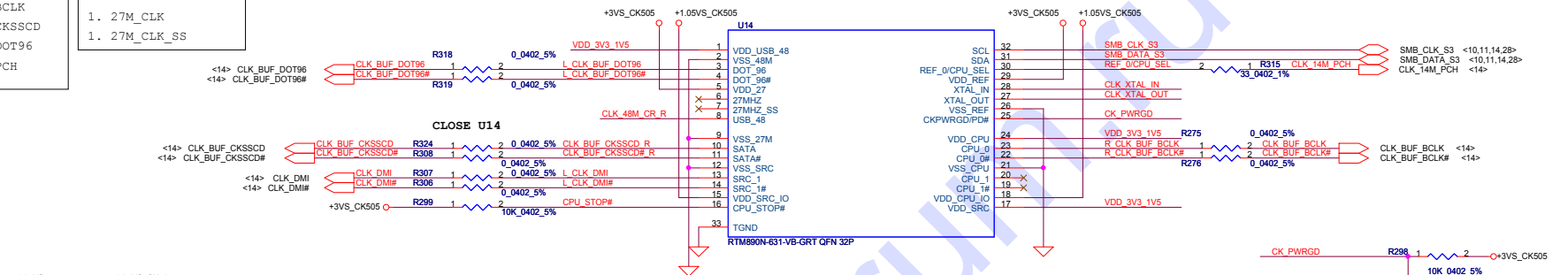
CLK GEN TO PCH

1. CLK_DMI
2. CLK_BUF_BCLK
3. CLK_BUF_CKSSCD
4. CLK_BUF_DOT96
5. CLK_14M_PCH

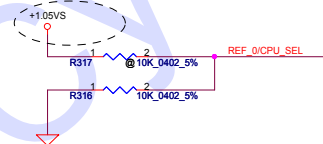
CLK GEN TO VGA

Unused

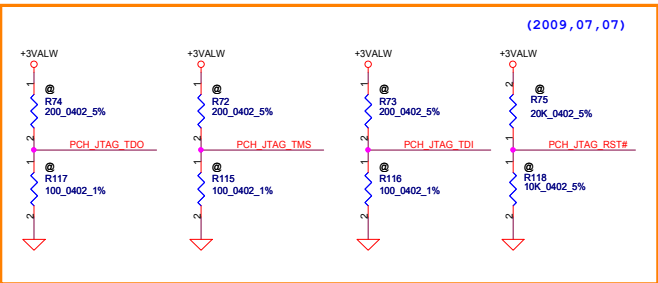
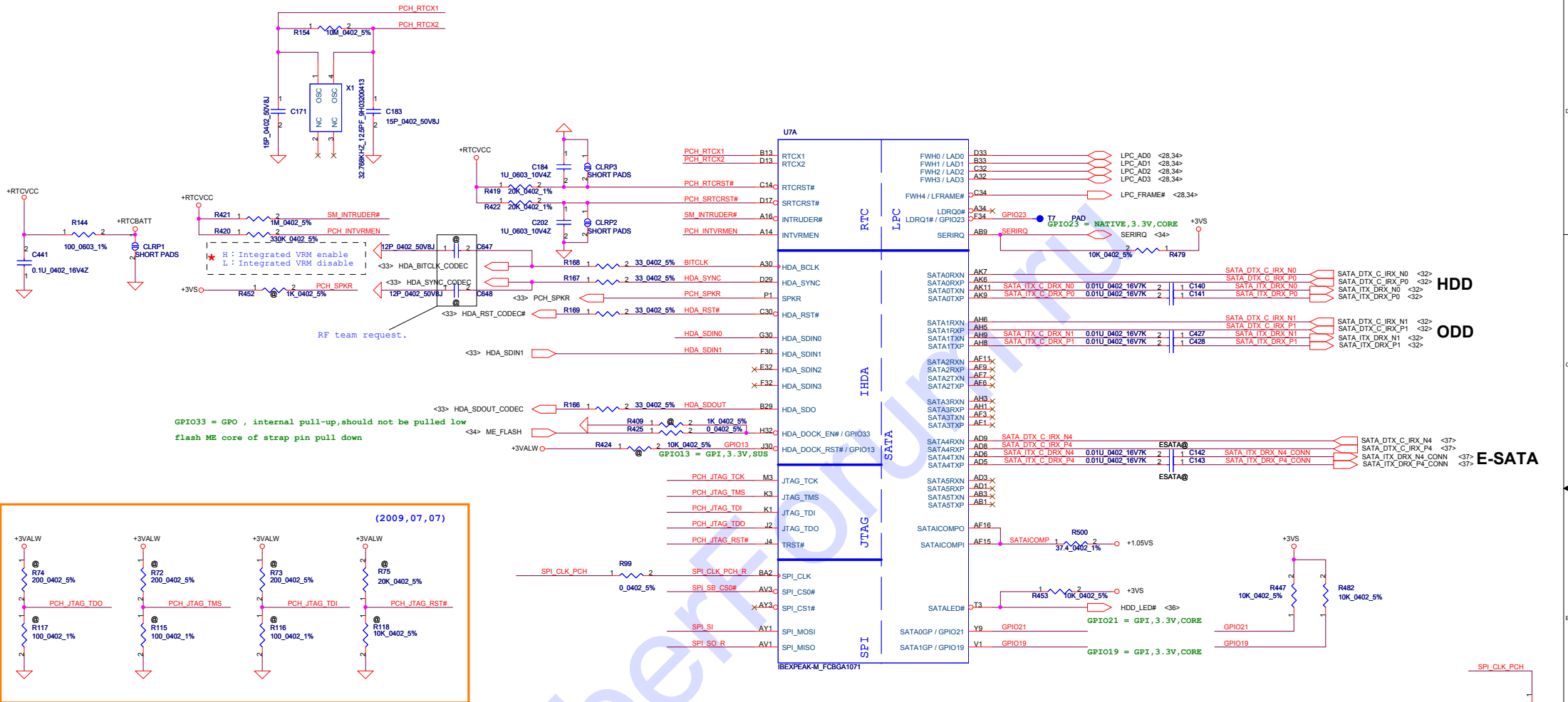
1. 27M_CLK
1. 27M_CLK_SS



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

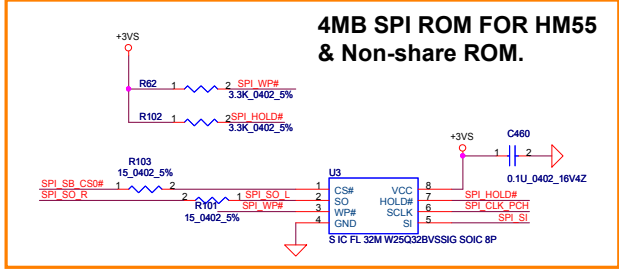


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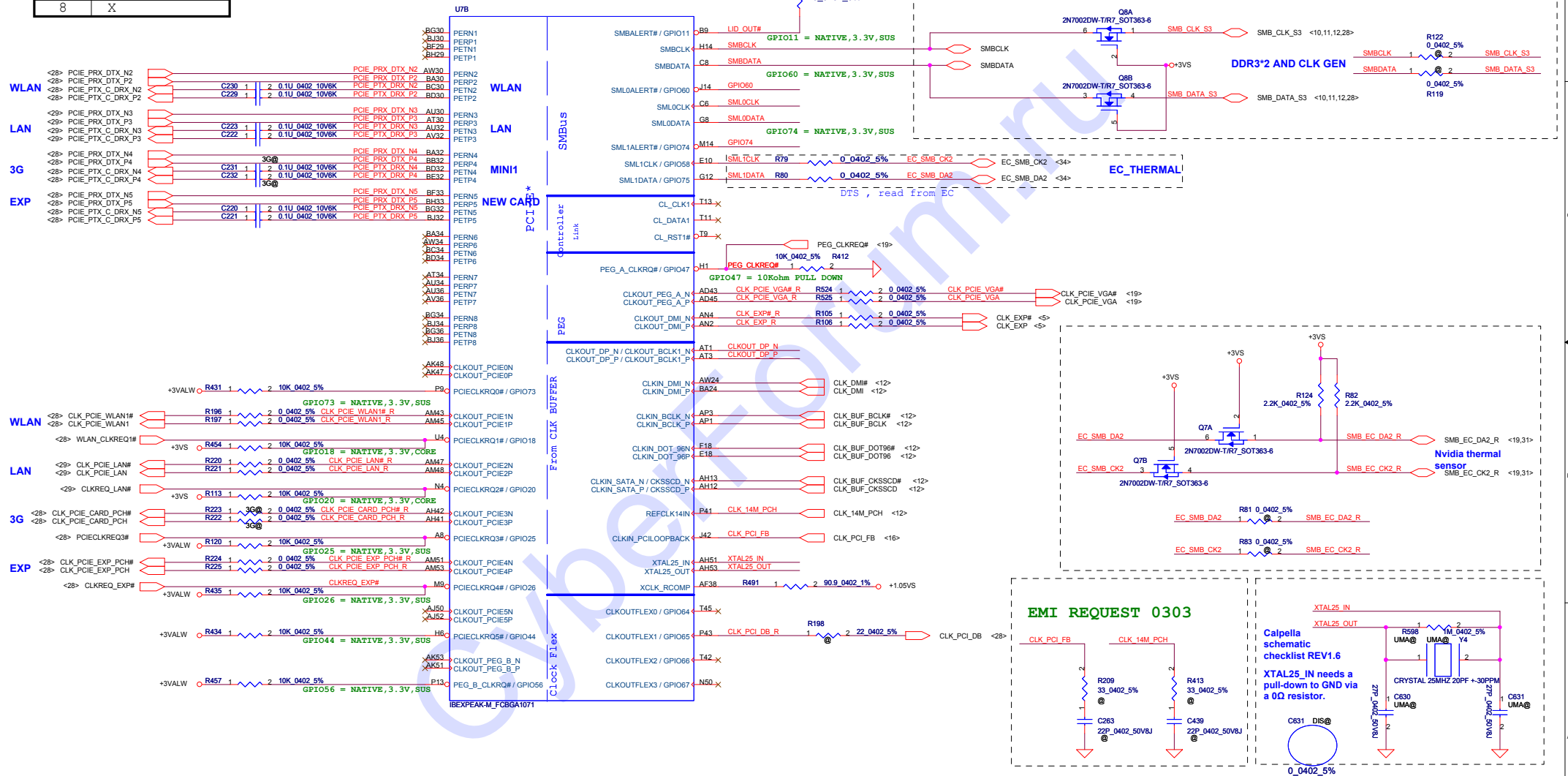
PCH Pin	RefDes	PCH JTAG Pre-Production		PCH JTAG Production
		ES1	ES2	MP
PCH_JTAG_TDO	R591	No Install	200ohm	No Install
PCH_JTAG_TMS	R590	No Install	100ohm	No Install
PCH_JTAG_TDI	R584	200ohm	200ohm	No Install
PCH_JTAG_TDO	R583	100ohm	100ohm	No Install
PCH_JTAG_TCK	R587	200ohm	200ohm	No Install
PCH_JTAG_TDI	R586	100ohm	100ohm	No Install
PCH_JTAG_TCK	R580	51ohm	51ohm	51ohm
PCH_JTAG_TMS	R595	20Kohm	20Kohm	No Install
PCH_JTAG_RST#	R594	10Kohm	10Kohm	No Install

PCH_JTAG_TCK R114 1 2 51.0K02.5% (2009,05,04)
FOR INTEL DPGD REV1.6 (MAY 2009)

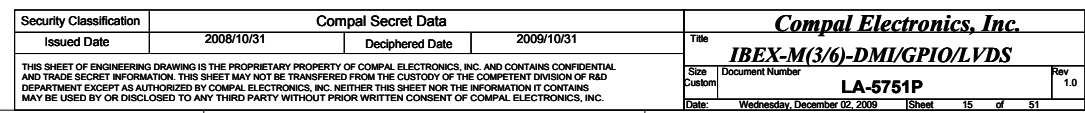


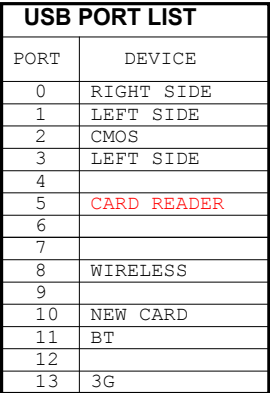
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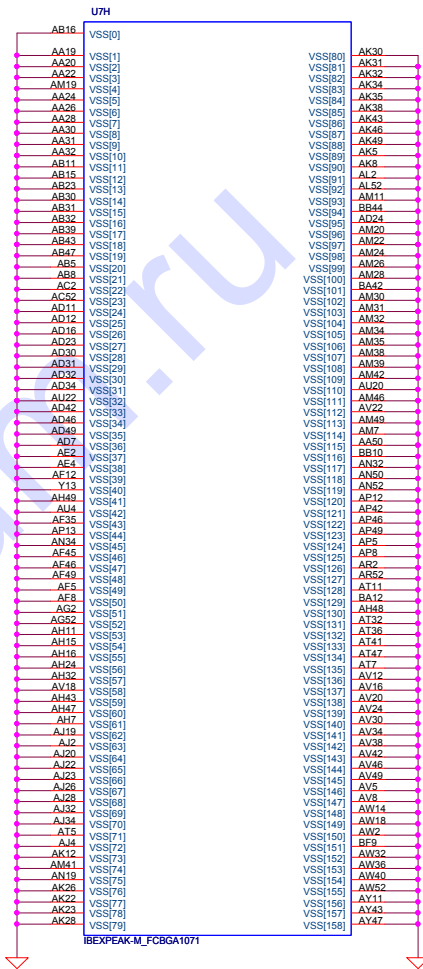
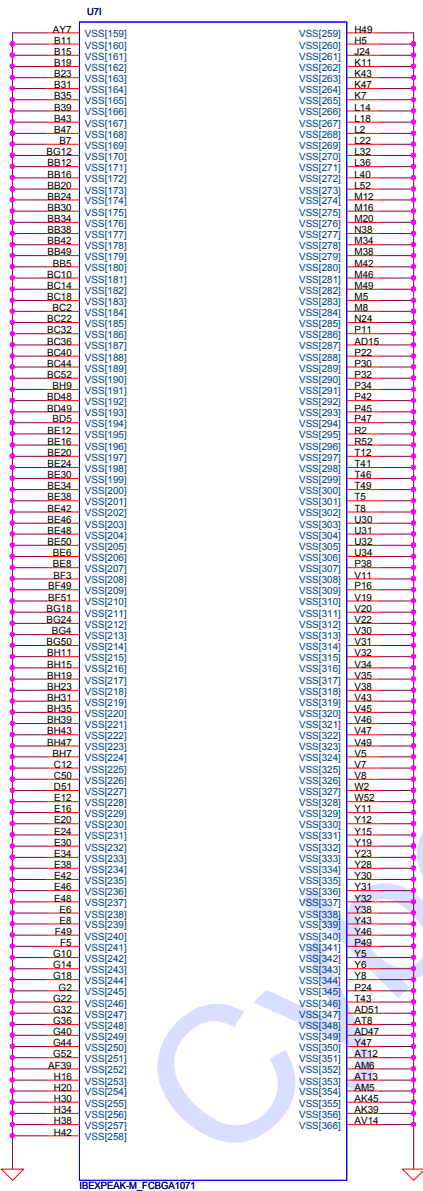
PCIE PORT LIST	
PORT	DEVICE
1	X
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	X
7	X
8	X



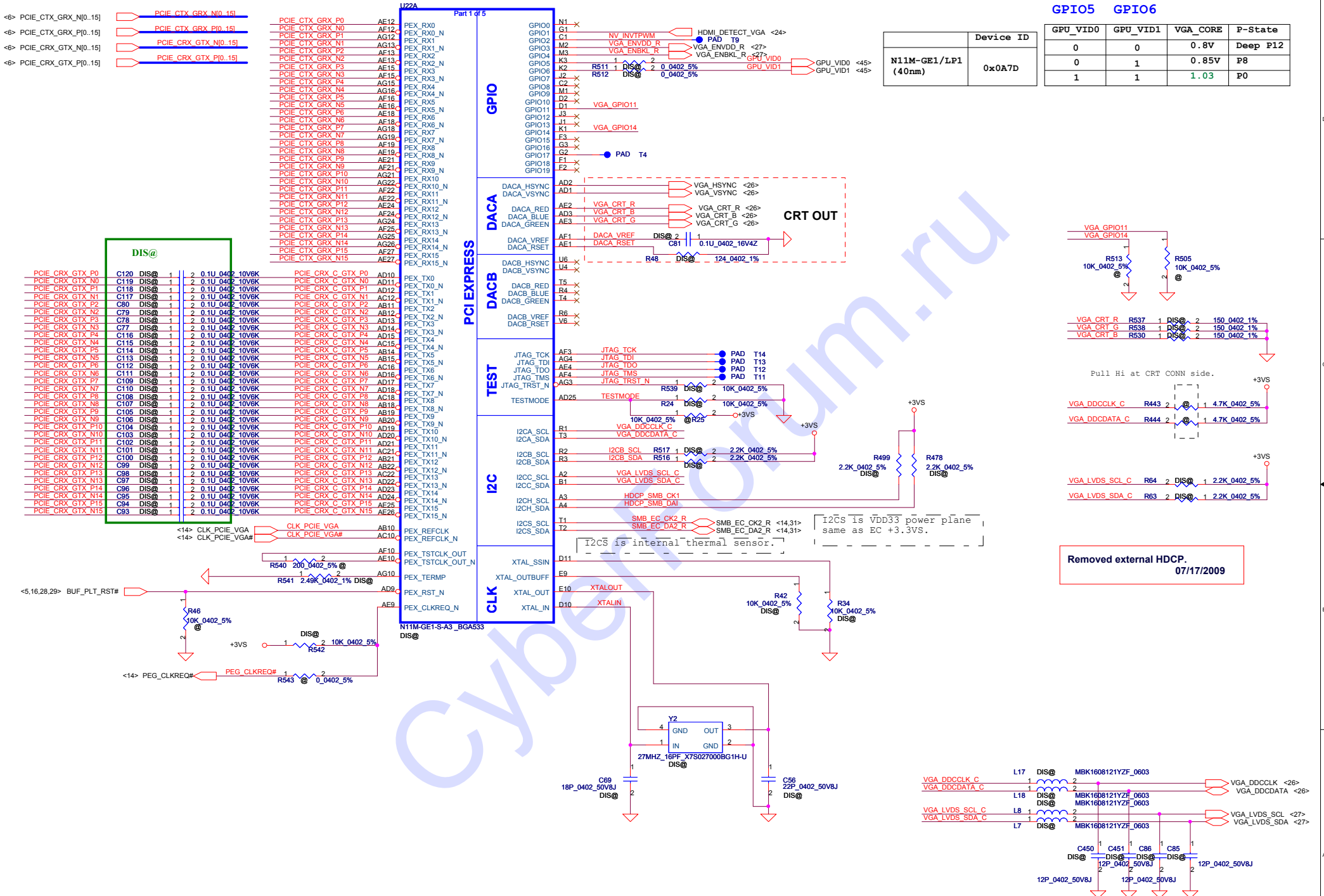
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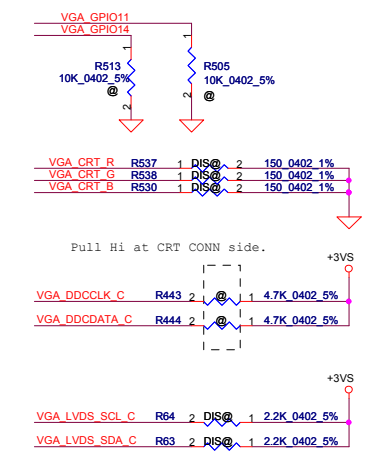


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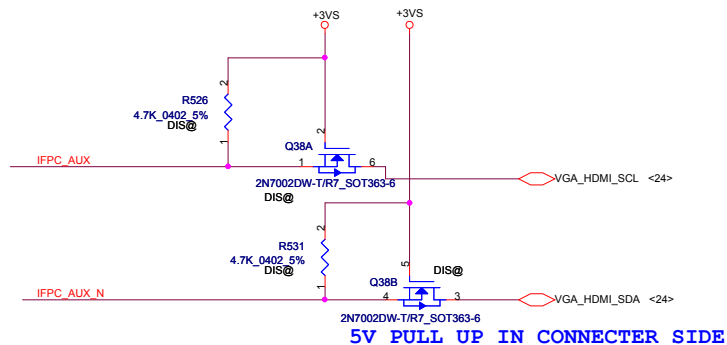
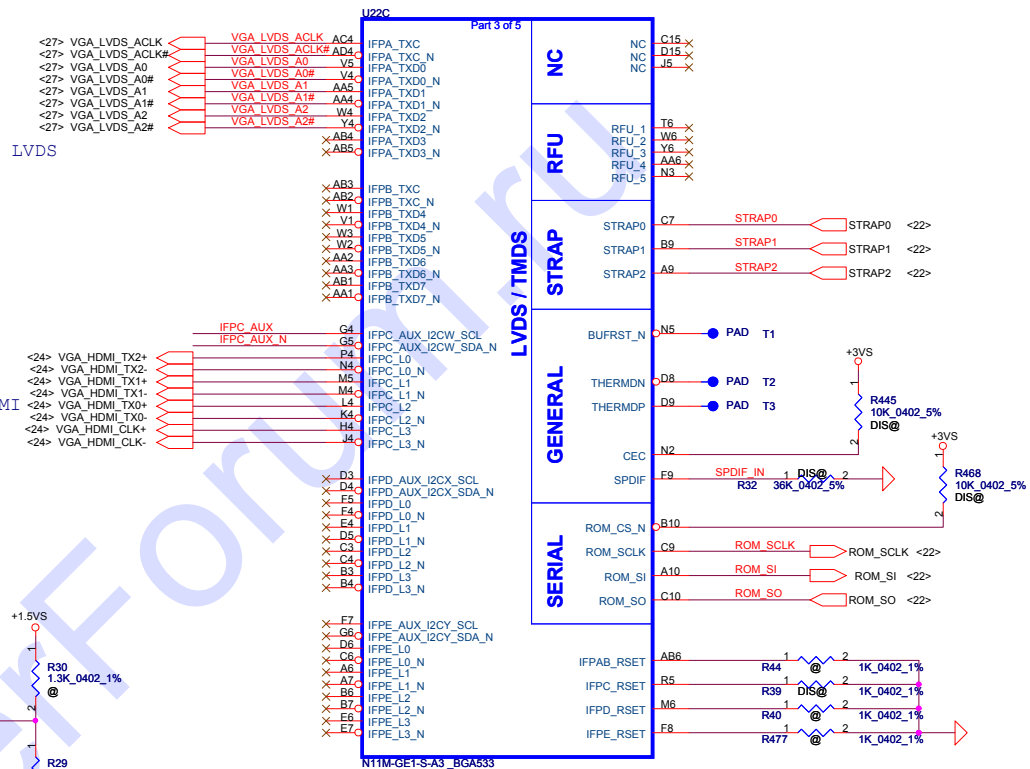
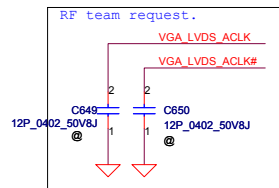
GPIO5		GPIO6		VGA_CORE		P-State
GPU_VID0	GPU_VID1	GPU_VID0	GPU_VID1	0.8V	0.85V	Deep P12
0	0	0	1	0.8V	0.85V	P8
0	1	1	1	1.03	1.03	P0

Device ID
0x0A7D

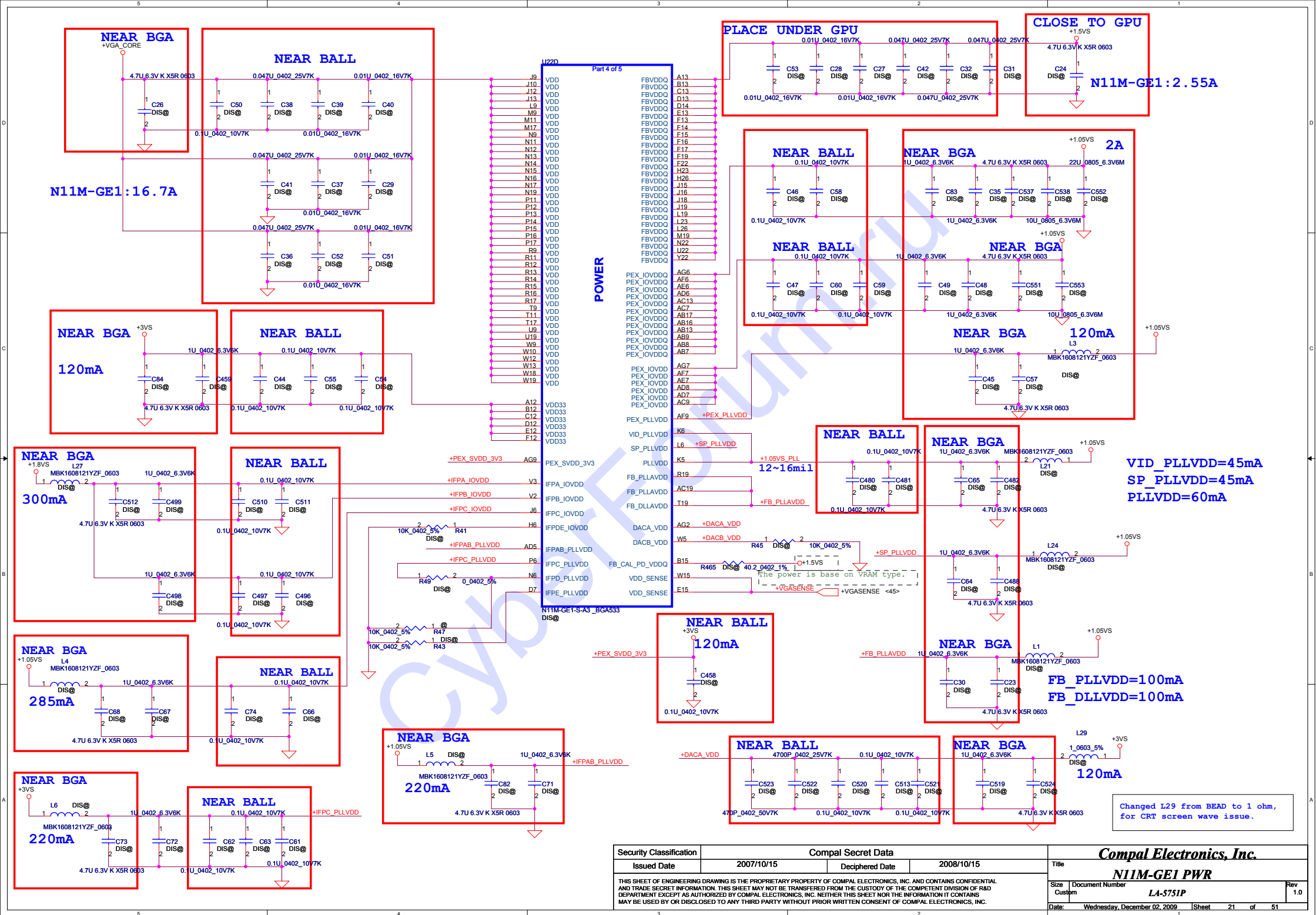


Removed external HDCP.
07/17/2009

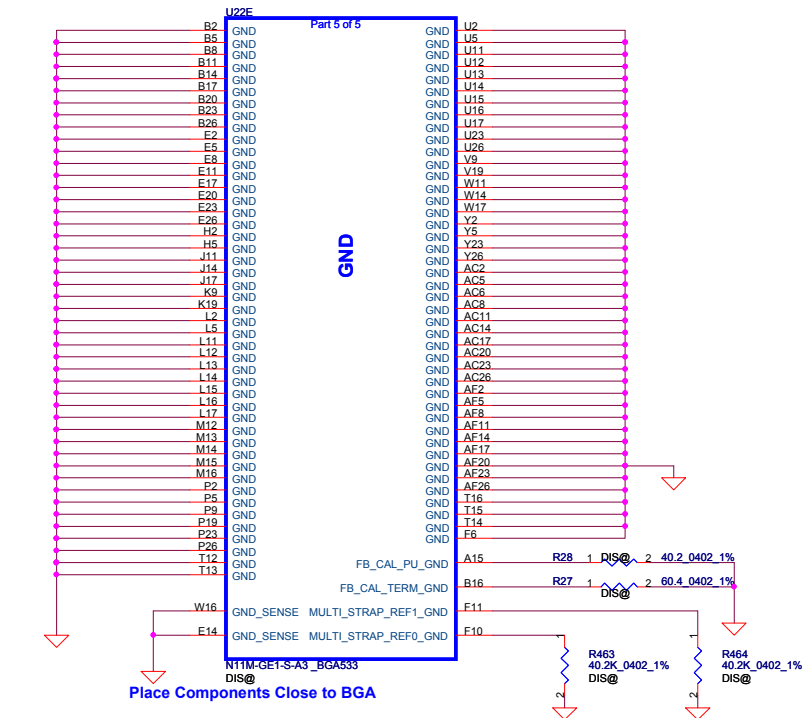
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	N11M-GE1 PCIE,GPIO,CLK	
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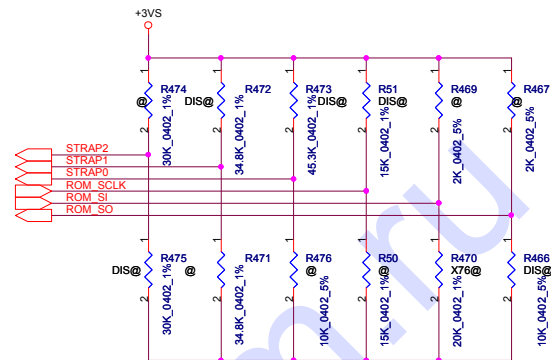
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				N11M-GE1 LVDS,Memory Bus	
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A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available



<20> STRAP2
<20> STRAP1
<20> STRAP0
<20> ROM_SCLK
<20> ROM_SI
<20> ROM_SO



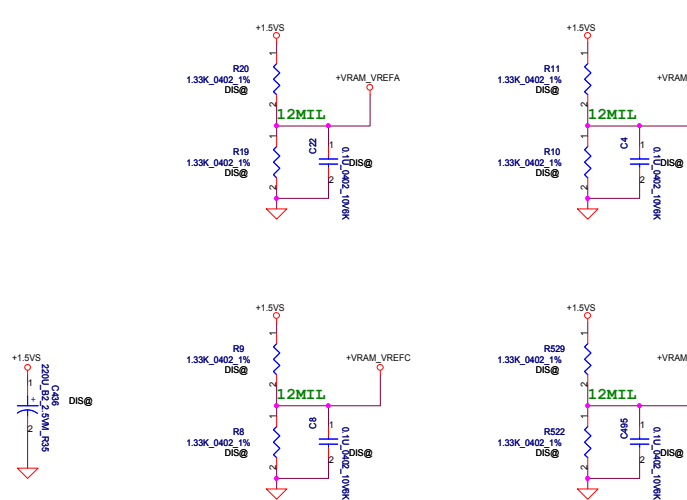
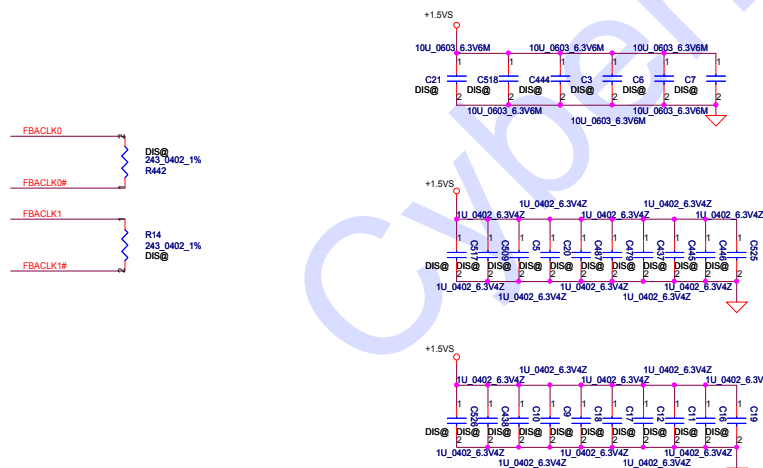
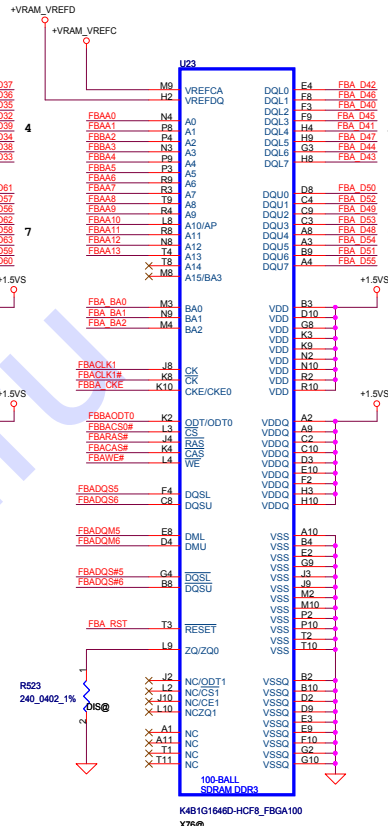
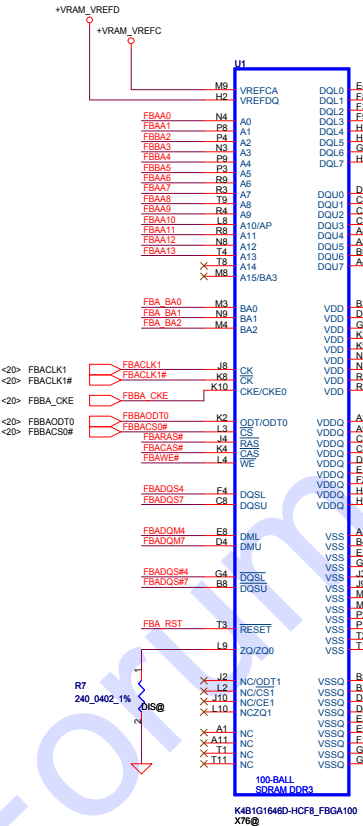
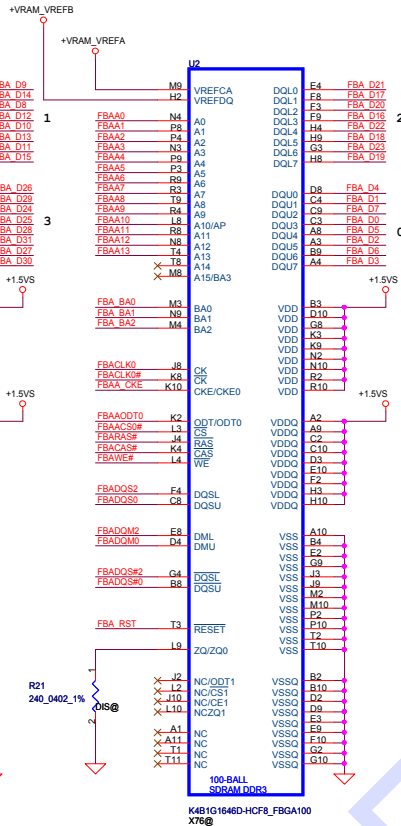
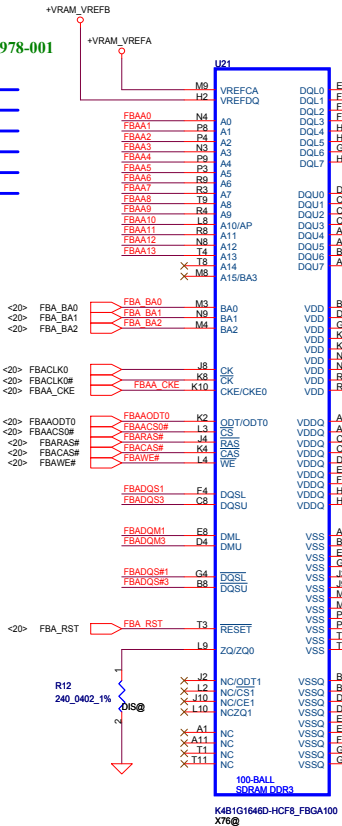
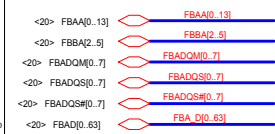
STRAP1 use for 3GIO_PADCFG to set 35K pull up.
(PUN-04335-001_V10 HW9 update)

GPU	FB Memory (DDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (default)	K4W1G1646E-HC12					
		64Mx16	PD 10K	PU 15K	PD 20K	PD 30K	PU 35K
	Hynix 800MHz	H5TQ1G63BFR-12C					
		64Mx16	PD 10K	PU 15K	PD 15K	PD 30K	PU 35K
X76							

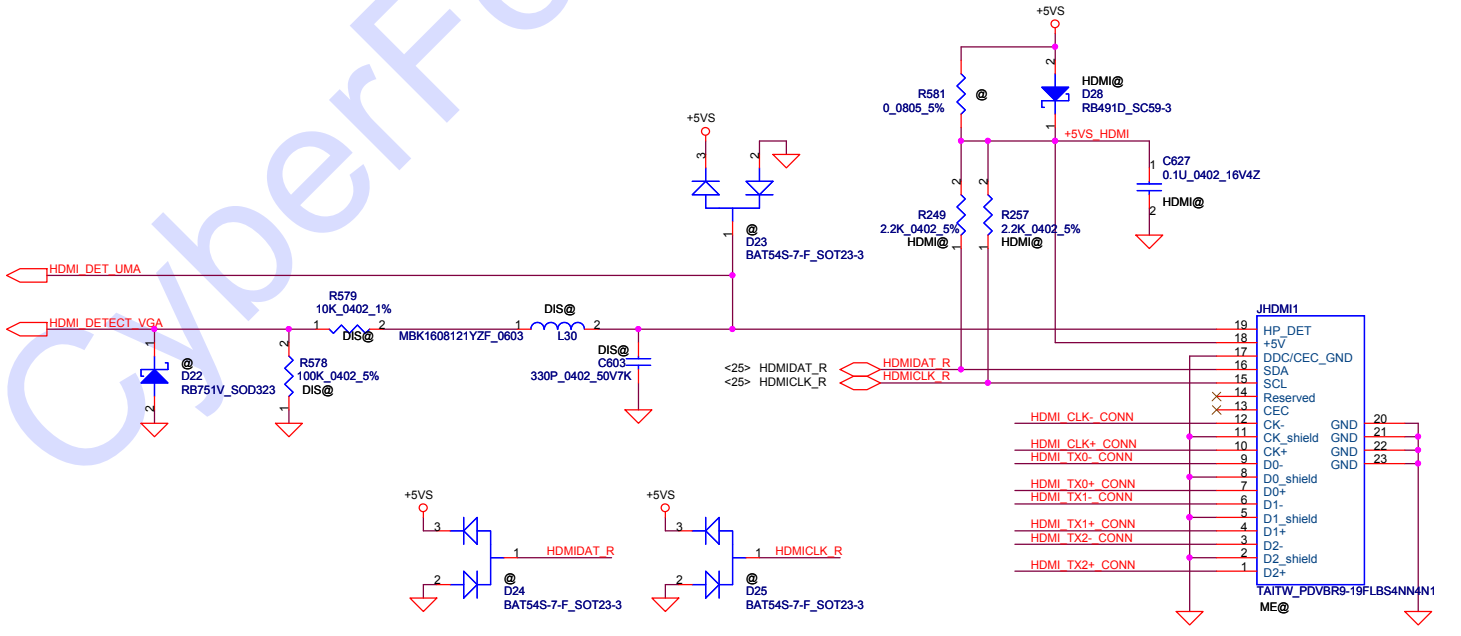
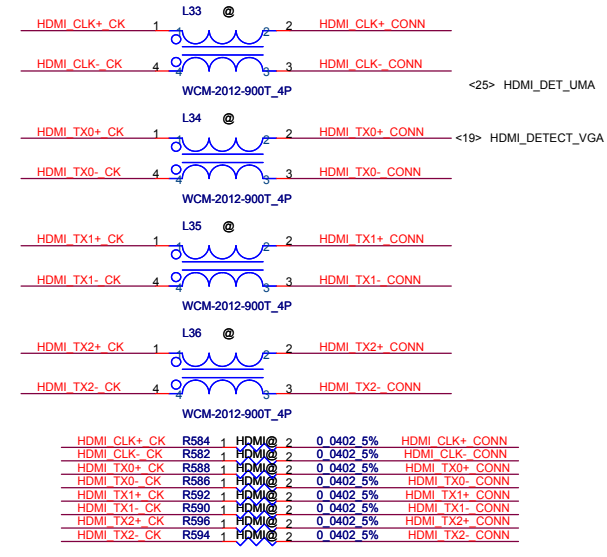
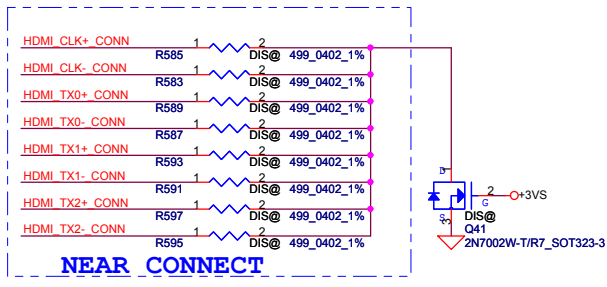
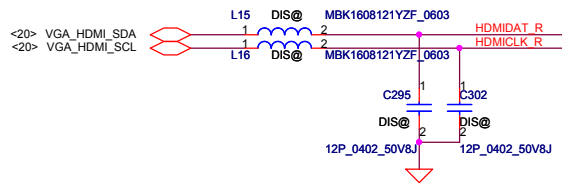
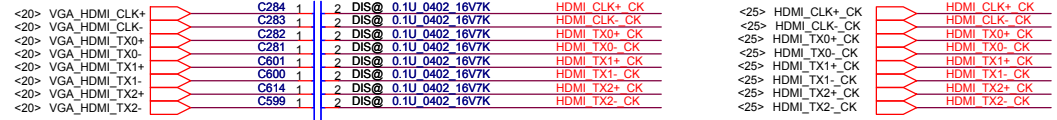
Must be used 1% resistor for driver calibration

DG-04642-001-V01(May 22, 2009)

N11x 40nm DDR3 MAPPING
NVIDIA COCUMENT FOR DA-3978-001

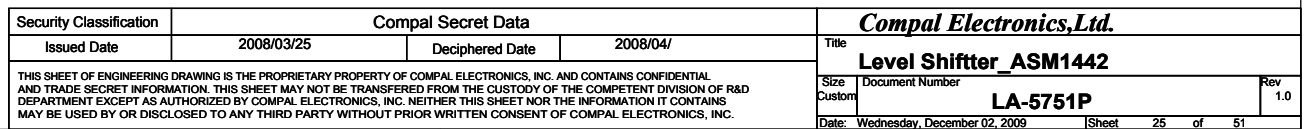


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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	
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Size	Custom	Document Number	LA-5751P	Date	Wednesday, December 02, 2009
Sheet	24	of	51	Rev	1.0

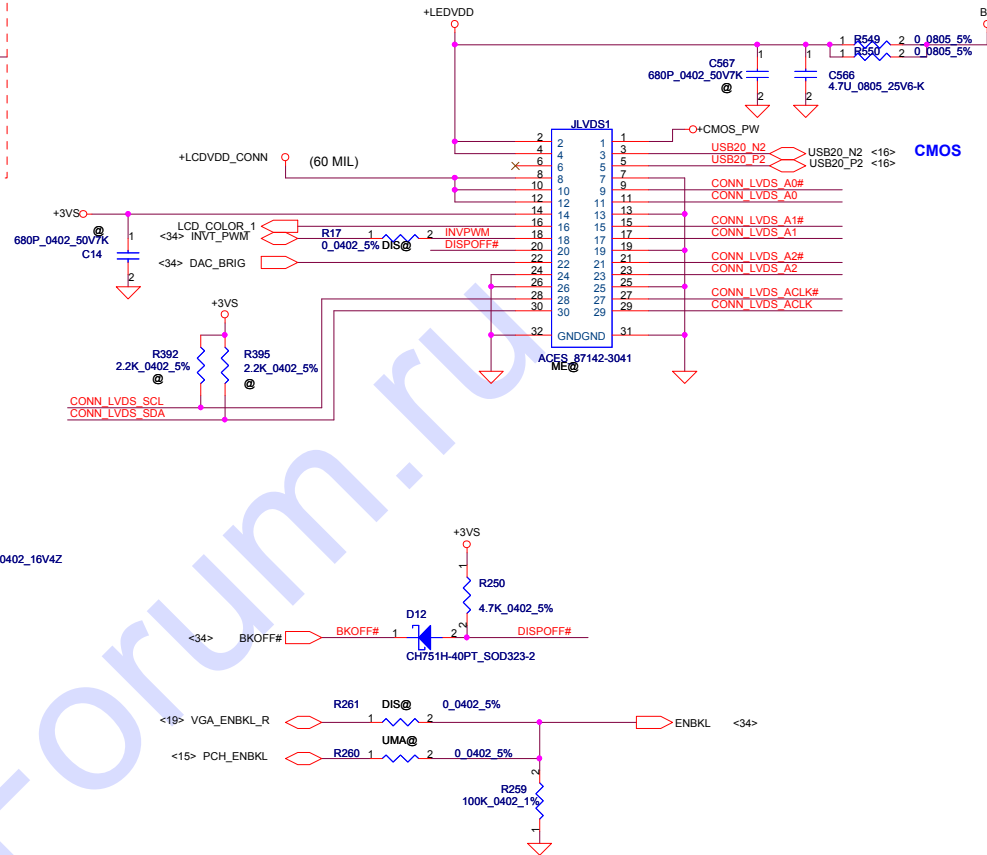
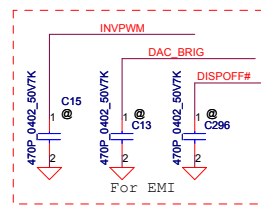
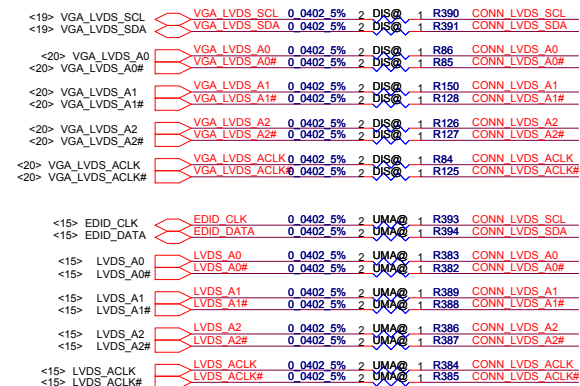
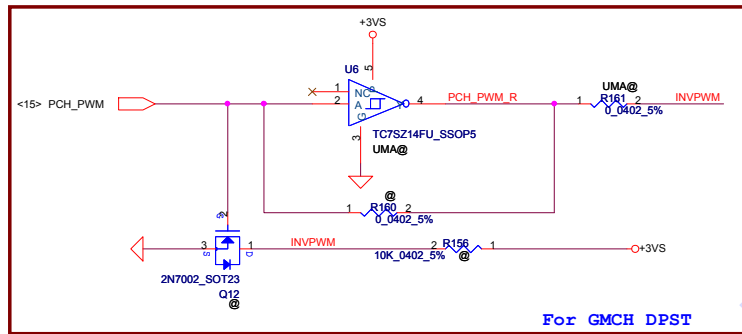
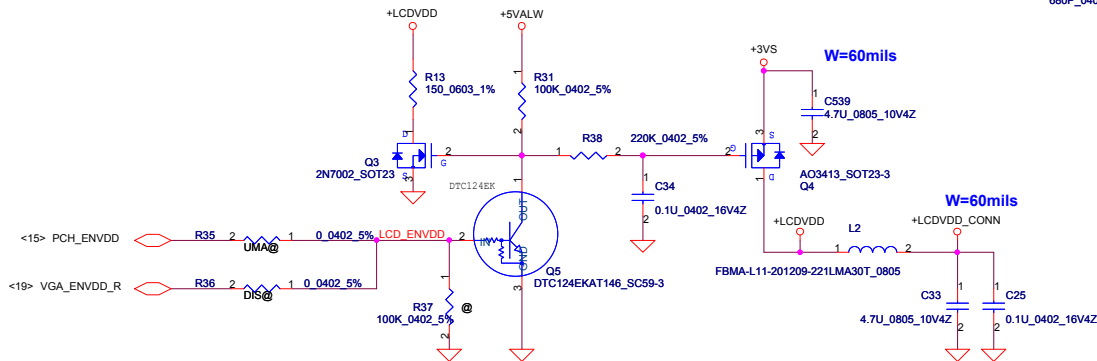
CHANGE R245 FROM 499 TO 3.4K OHM



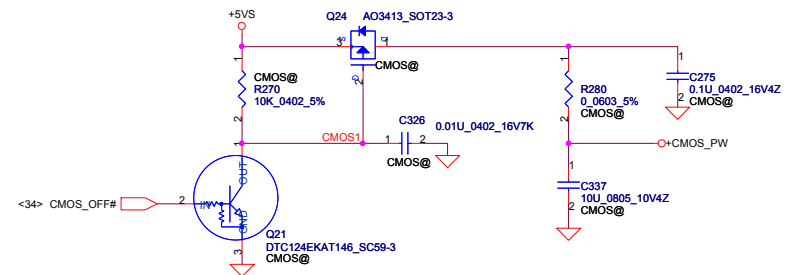


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				Document Number	1.0
				Custom	LA-5751P
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LCD POWER CIRCUIT



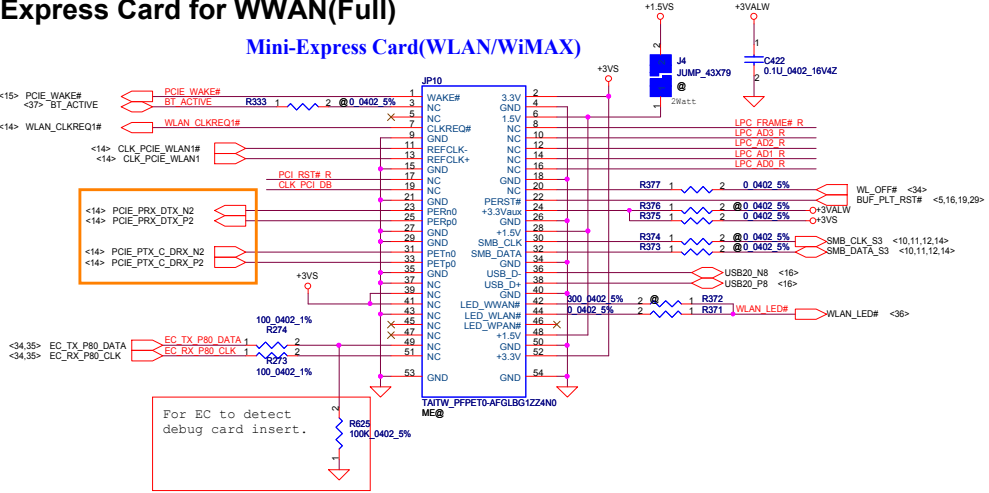
CMOS Camera



Security Classification		Compal Secret Data		Compal Electronics, Inc. LVDS/CAMERA	
Issued Date	2007/10/15	Deciphered Date	2008/10/15		
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				LA-5751P Date: Wednesday, December 02, 2009 Sheet 27 of 51	
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Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for WWAN(Full)

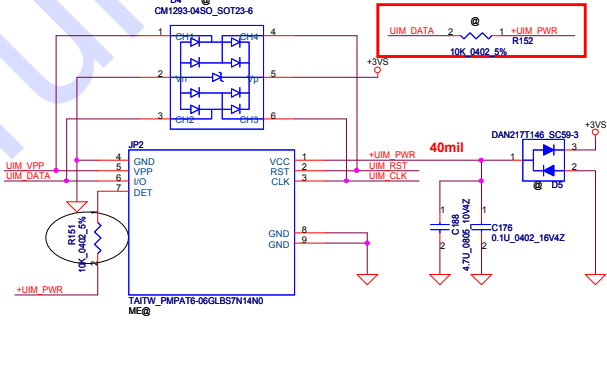
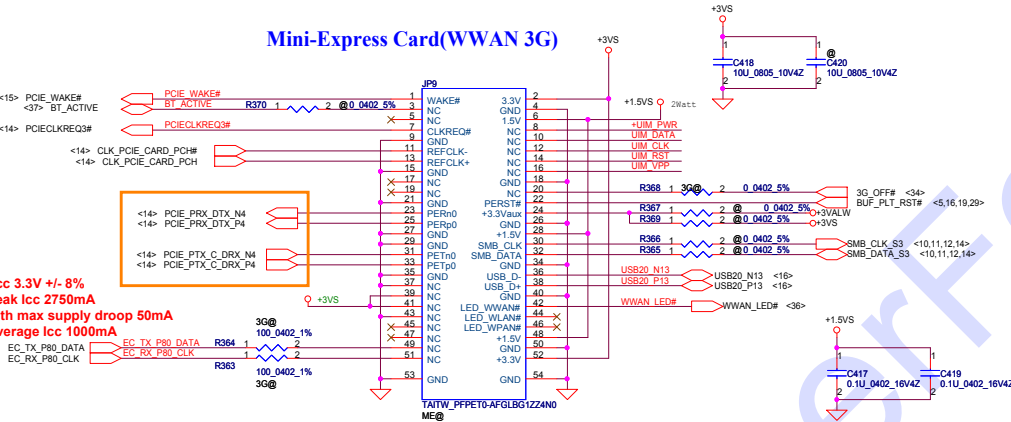
Mini-Express Card(WLAN/WiMAX)



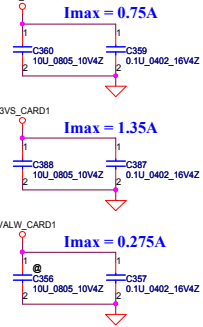
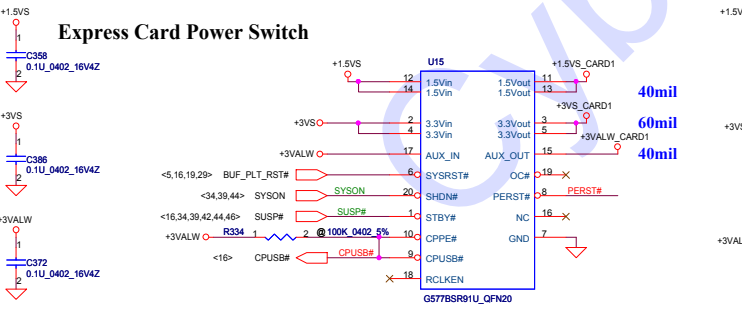
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R284	1	2	0.0402 5%	LPC_FRAME#	LPC_FRAME#	<13,34>
LPC_AD3 R	R285	1	2	0.0402 5%	LPC_AD3	LPC_AD3	<13,34>
LPC_AD2 R	R286	1	2	0.0402 5%	LPC_AD2	LPC_AD2	<13,34>
LPC_AD1 R	R287	1	2	0.0402 5%	LPC_AD1	LPC_AD1	<13,34>
LPC_AD0 R	R288	1	2	0.0402 5%	LPC_AD0	LPC_AD0	<13,34>
PCI_RST# R	R290	1	2	0.0402 5%	PCI_RST#	PCI_RST#	<13,34>
CLK_PCI_DB	R290	1	2	0.0402 5%	CLK_PCI_DB	CLK_PCI_DB	<14>

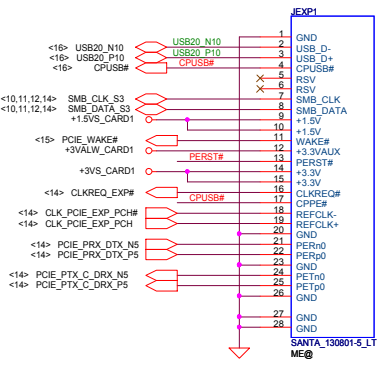
Mini-Express Card(WWAN 3G)

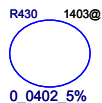


Express Card Power Switch



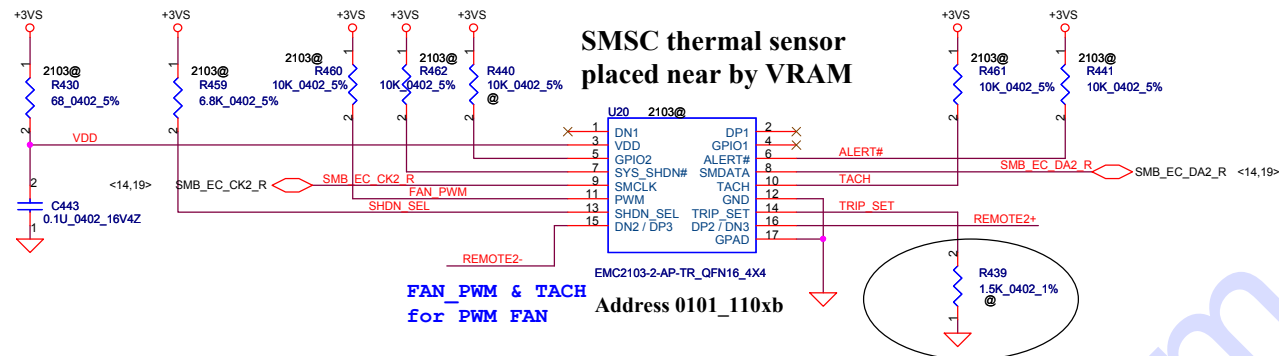
New Card 34mm Socket (Left/TOP)





1403:
@C508/@C324=100p

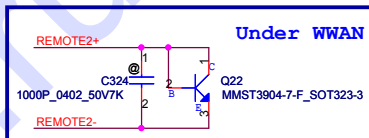
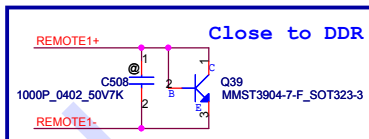
SMSC thermal sensor placed near by VRAM



FAN_PWM & TACH
for PWM FAN

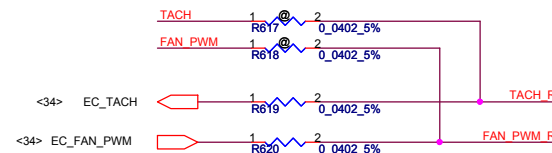
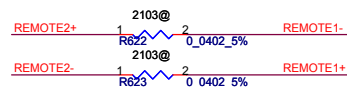
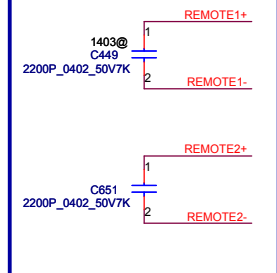
Address 0101_110xb

internal pull up 1.2K to 1.5V
R for initial thermal
shutdown temp

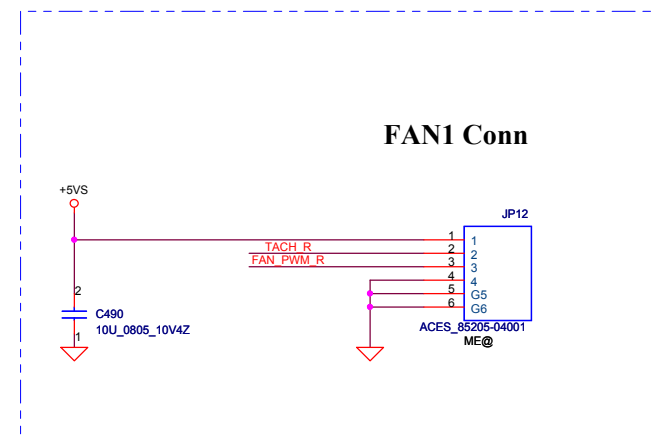


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

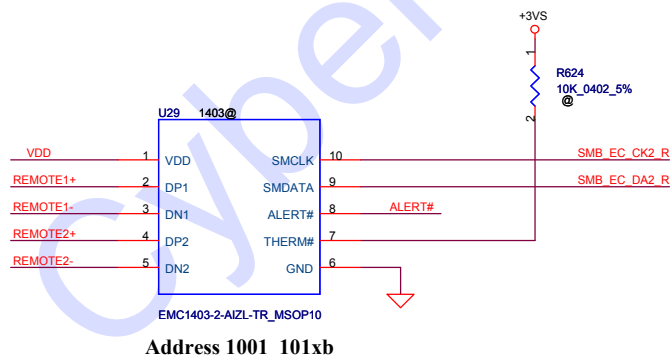
Close U20



FAN1 Conn

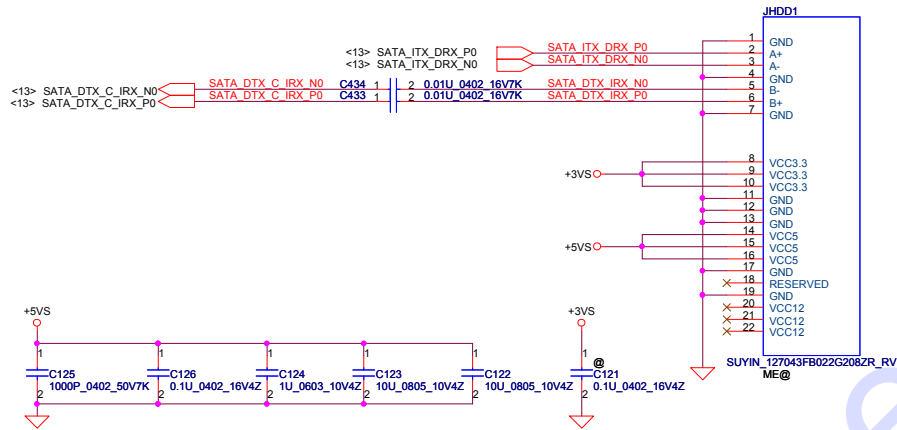


Shutdown Temp	TRIP_SET R439 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm

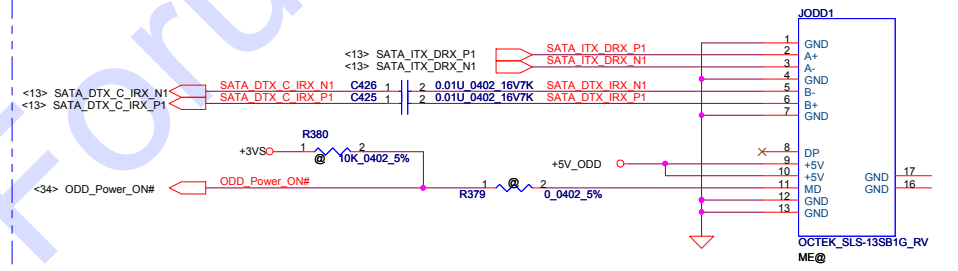


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				Date: Wednesday, December 02, 2009	Sheet 31 of 51

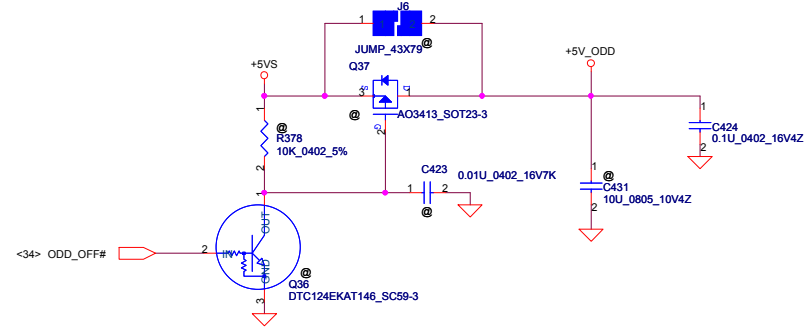
SATA HDD Conn.



SATA ODD Conn.

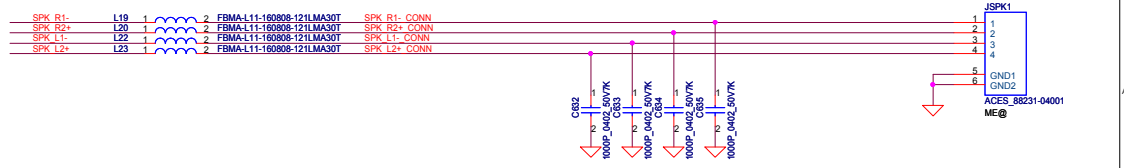
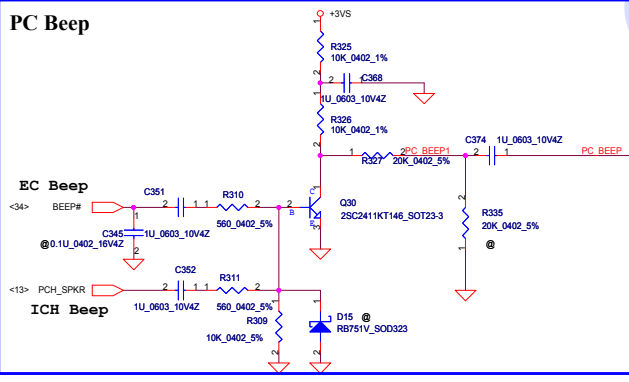
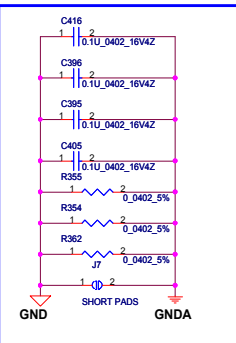
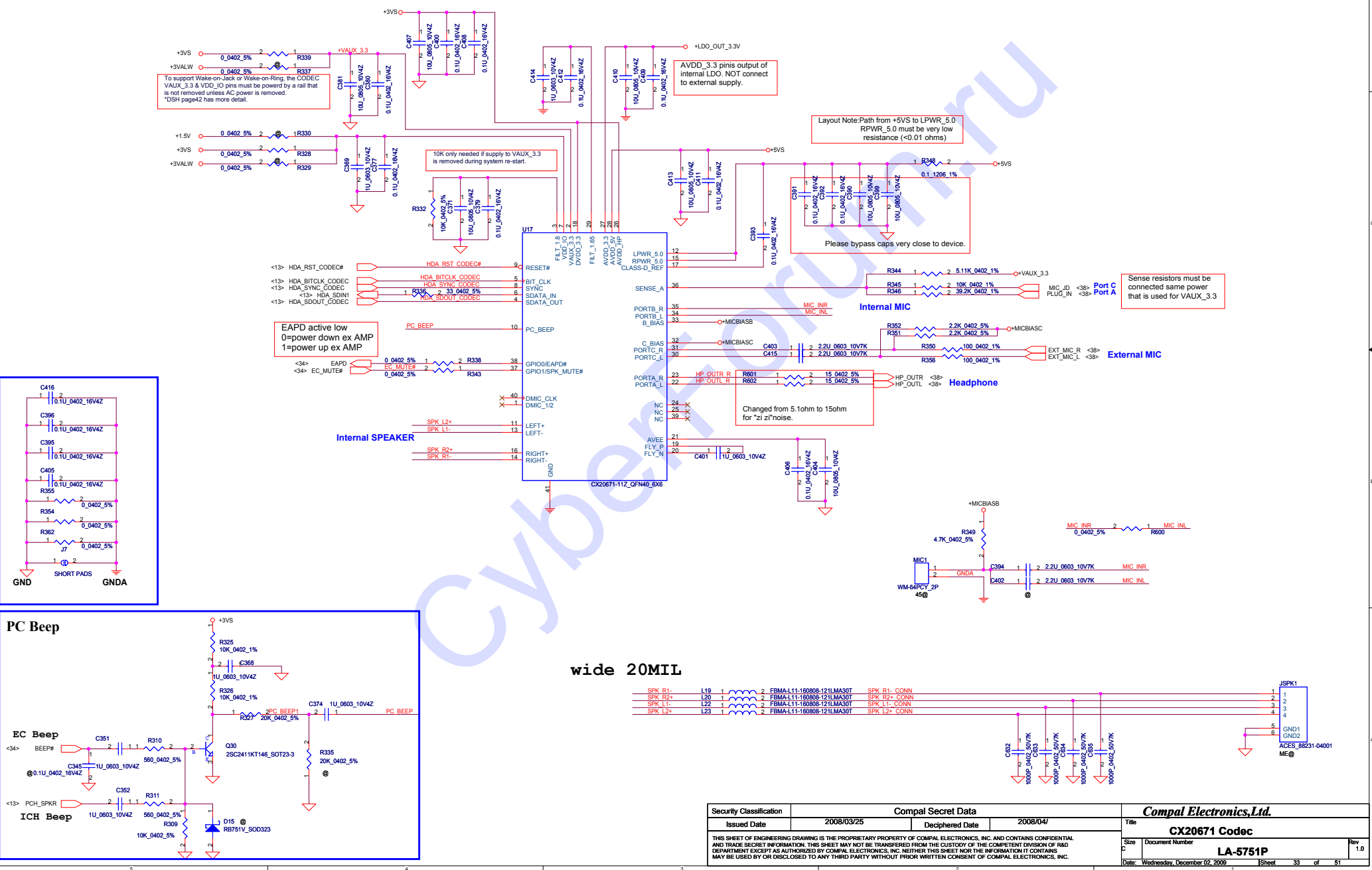


ODD Power Control

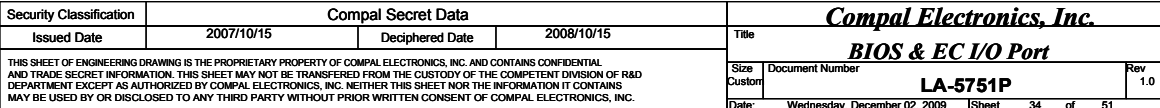


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CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO) .
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO) .

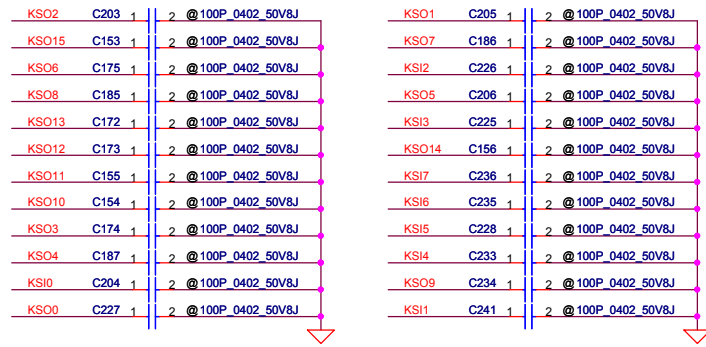


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Size	Document Number	Rev		
C	LA-5751P	1.0		
Date: Wednesday, December 02, 2009		Sheet	33	of 51



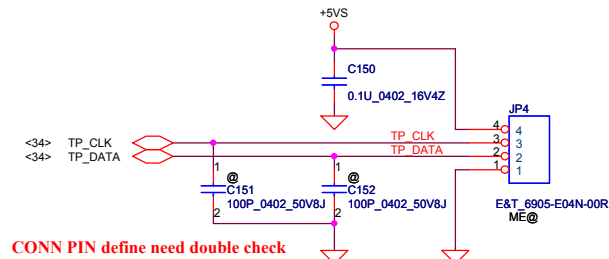
INT_KBD Conn.

KSI[0..7] <34>
KSO[0..15] <34>

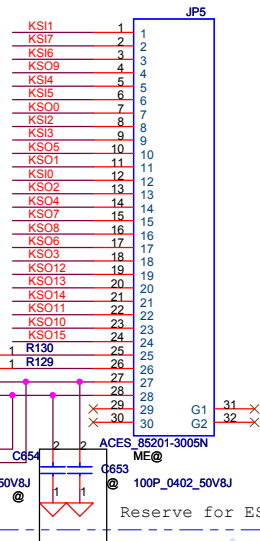


CONN PIN define need double check

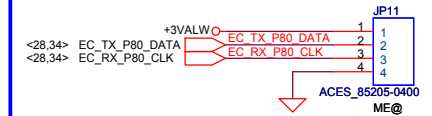
To TP/B Conn.



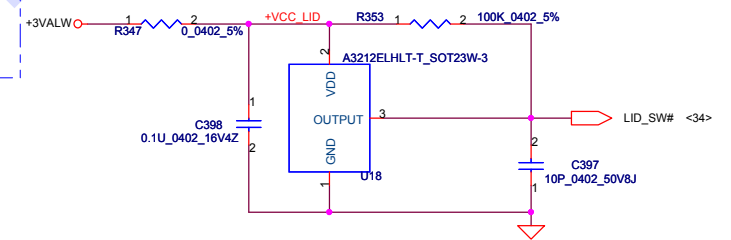
CONN PIN define need double check



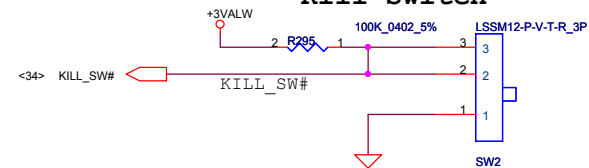
EC DEBUG PORT



Lid Switch



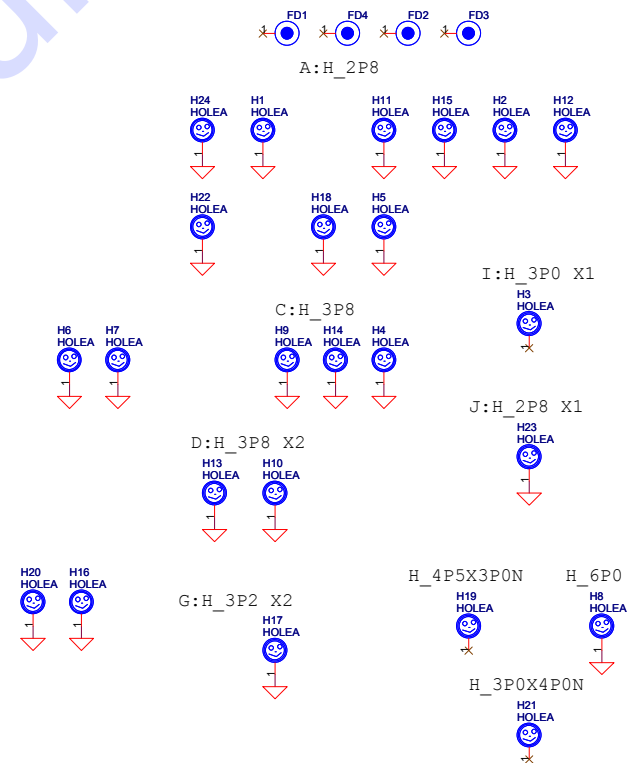
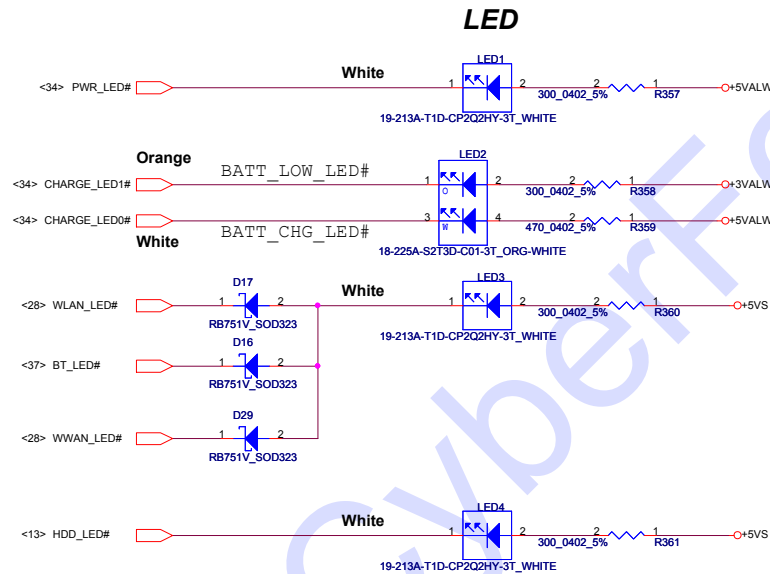
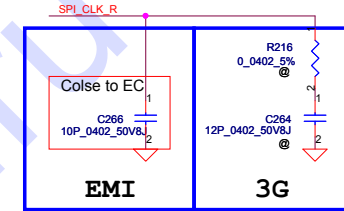
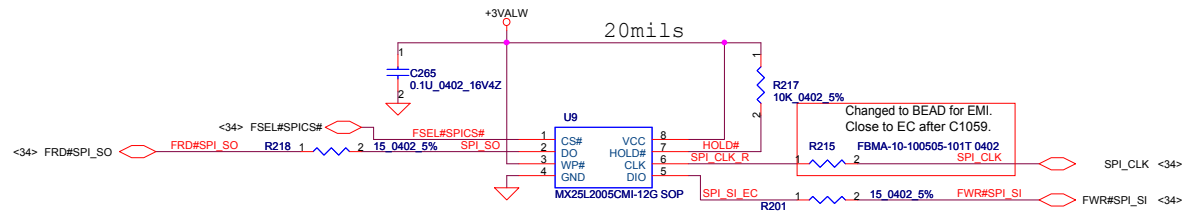
Kill Switch



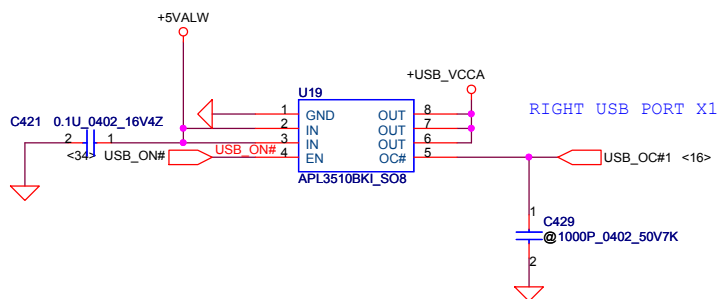
Kill

STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

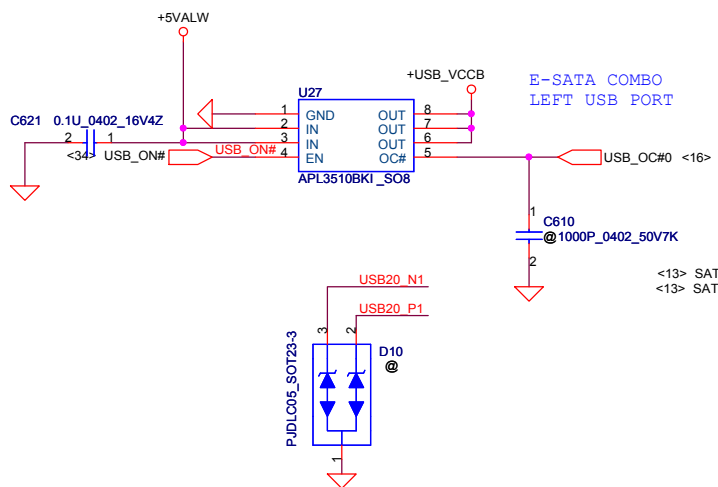
FOR EC 256KB SPI ROM (150mil PACKAGE)



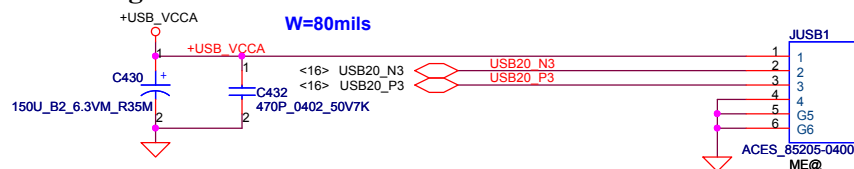
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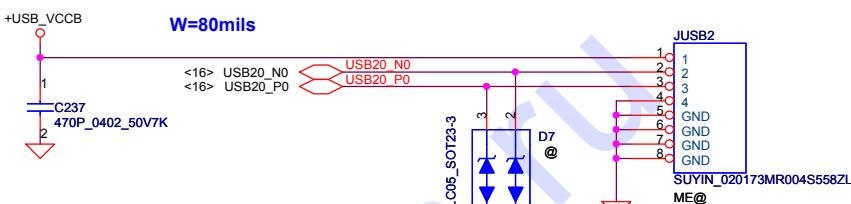
U19/U27 USB power switch need update symbol to SA000039E00(Low enable)



Right USB Conn.

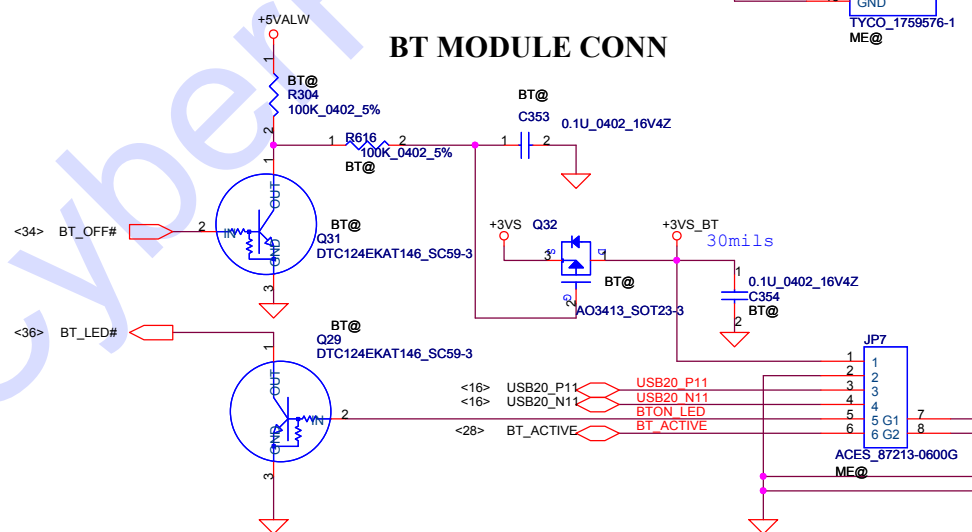


Left USB Conn.



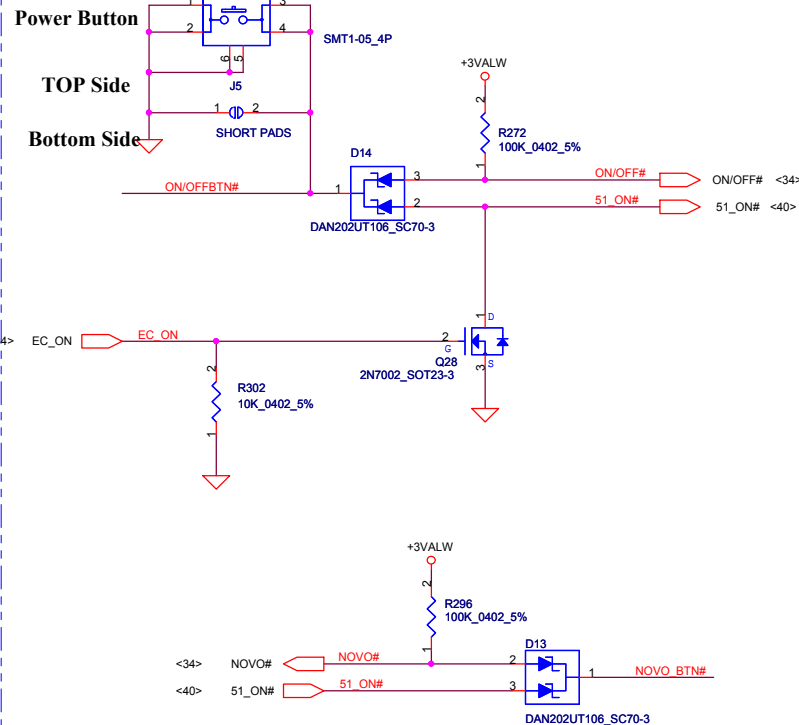
USB
A+ = RXP
A- = RXN
B- = TXN
B+ = TXP

BT MODULE CONN

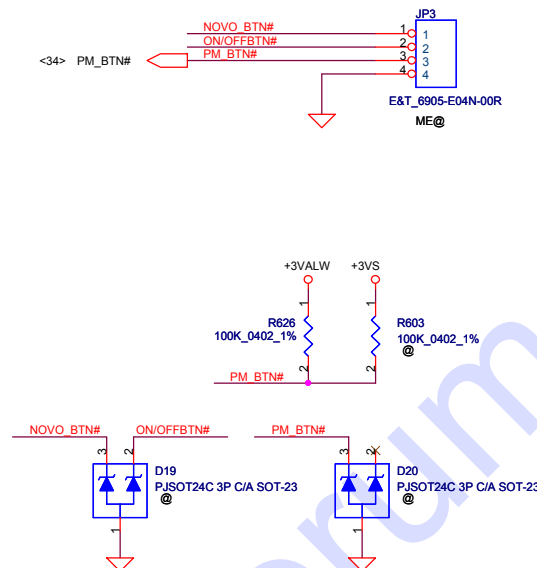


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ON/OFF switch

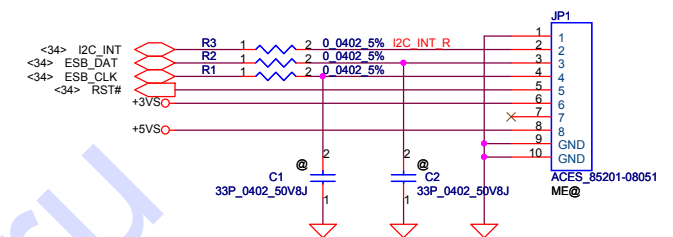


Power Bottom Board Conn. 4pin

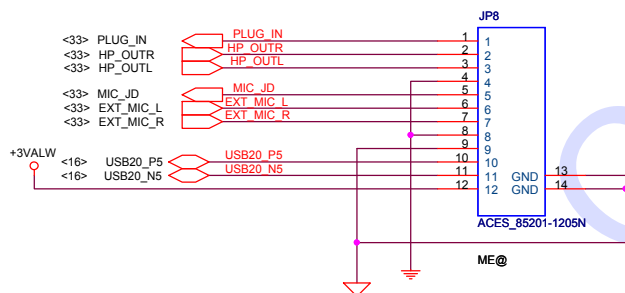


Cap Sensor Board Conn. 6pin

ENE SB3534

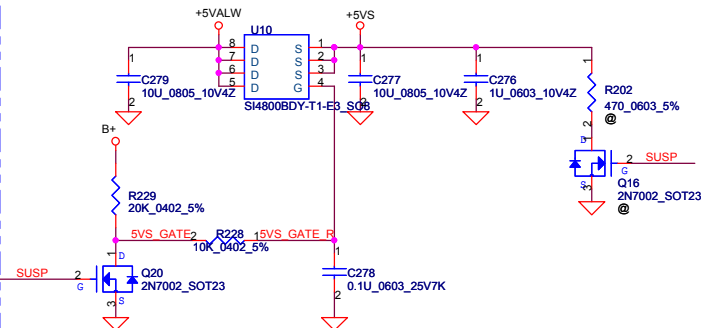


Card Reader/Audio Jack SB CONN

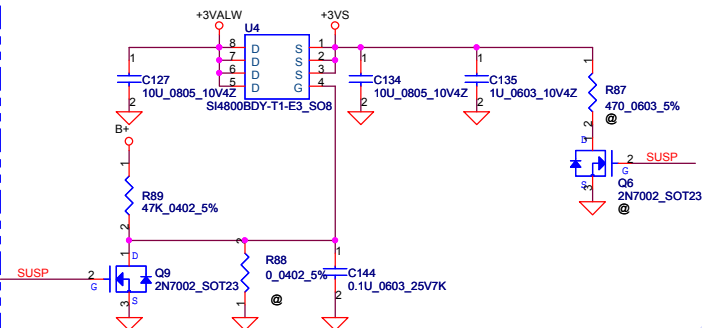


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				Size Custom
				Document Number
				LA-5751P
				Rev 1.0
				Date: Wednesday, December 02, 2009
				Sheet 38 of 51

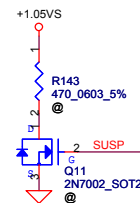
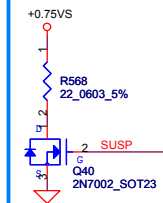
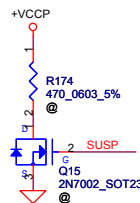
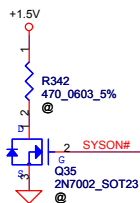
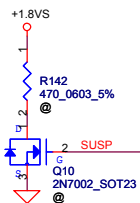
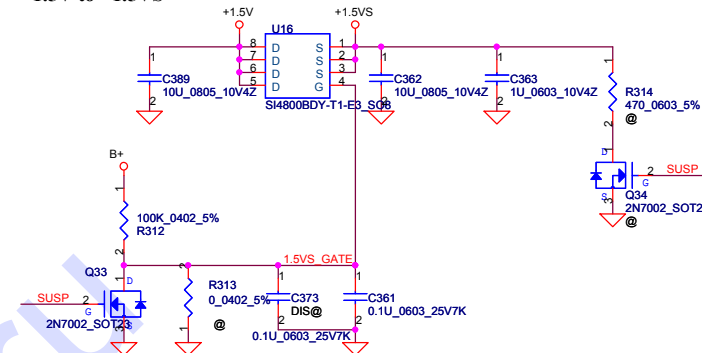
+5VALW TO +5VS



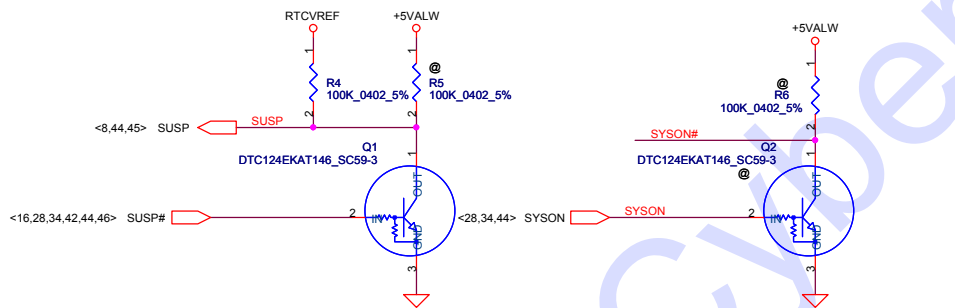
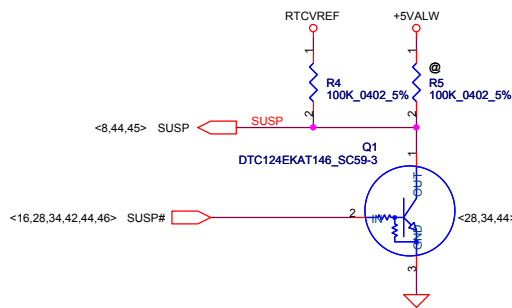
+3VALW TO +3VS



+1.5V to +1.5VS

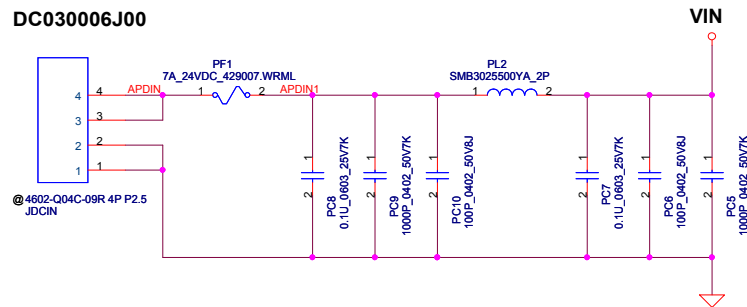


For Intel S3 Power Reduction.



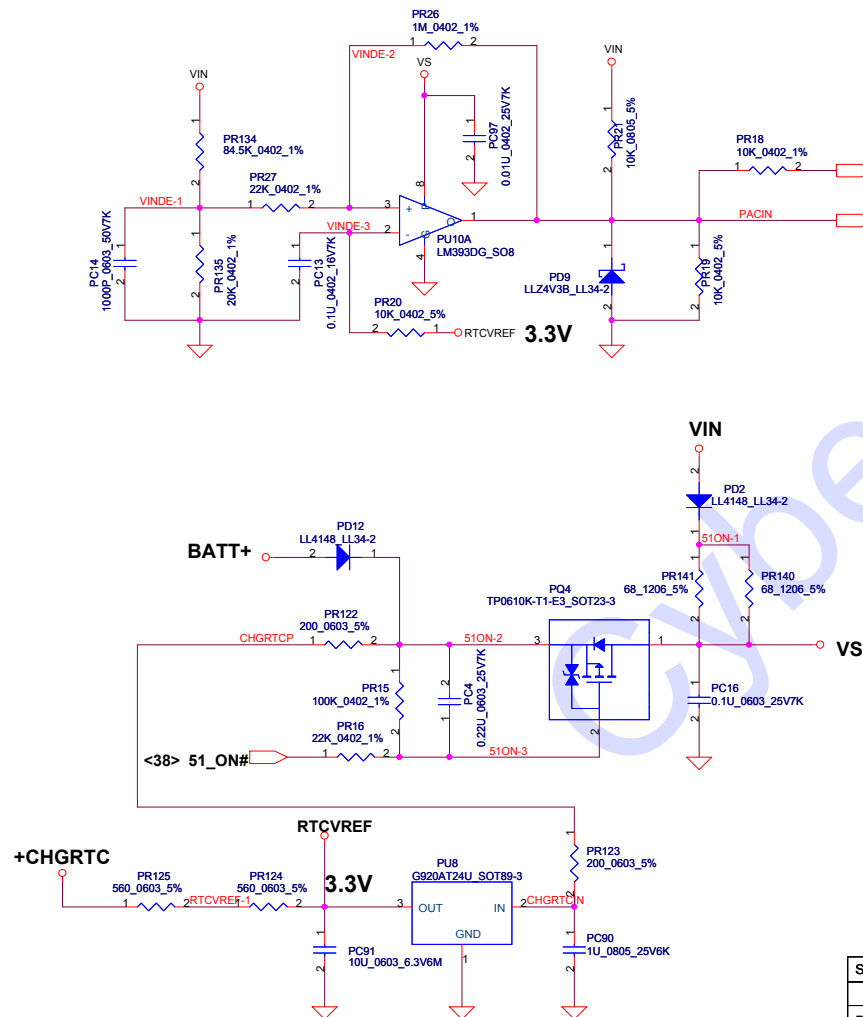
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				Size	Document Number	Rev
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DC030006J00



Vin Detector

	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V



ACIN

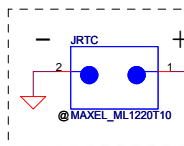
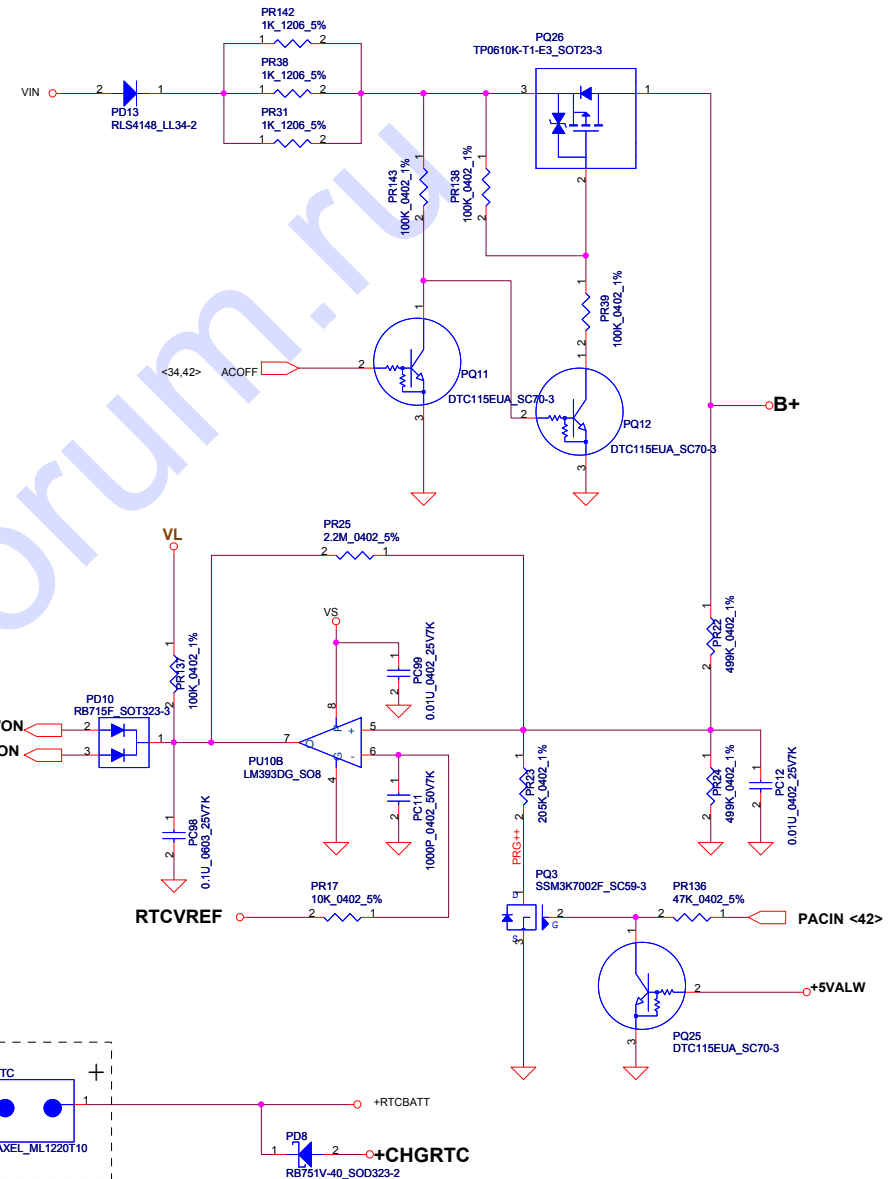
Precharge detector

	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector

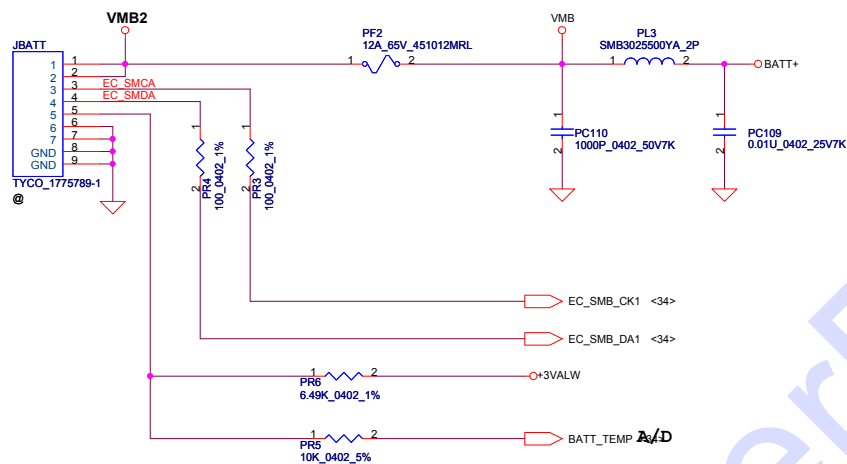
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



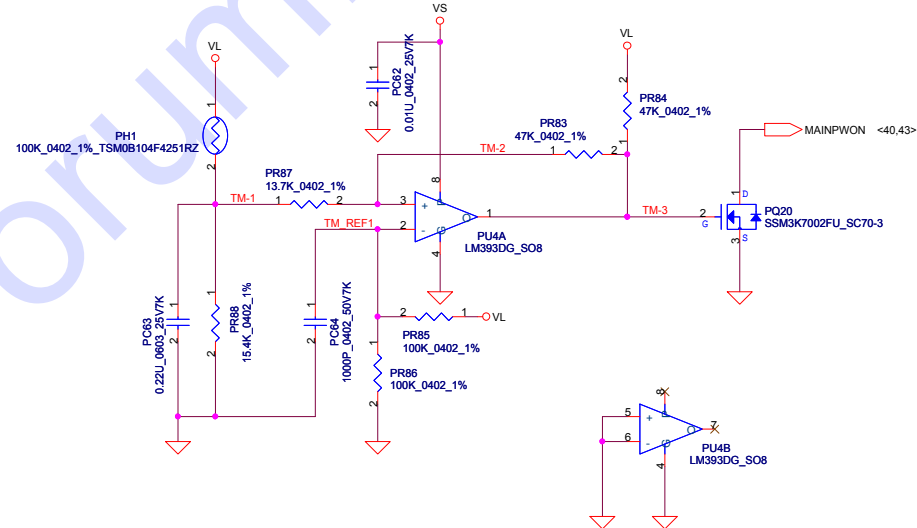
RTC Battery

Security Classification				Compal Secret Data				Compal Electronics, Inc.		
Issued Date				2009/01/06				Title		
Deciphered Date				2010/01/06				DCIN & DETECTOR		
Size				Document Number				Rev		
Custom								1.0		
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								40 of 51		

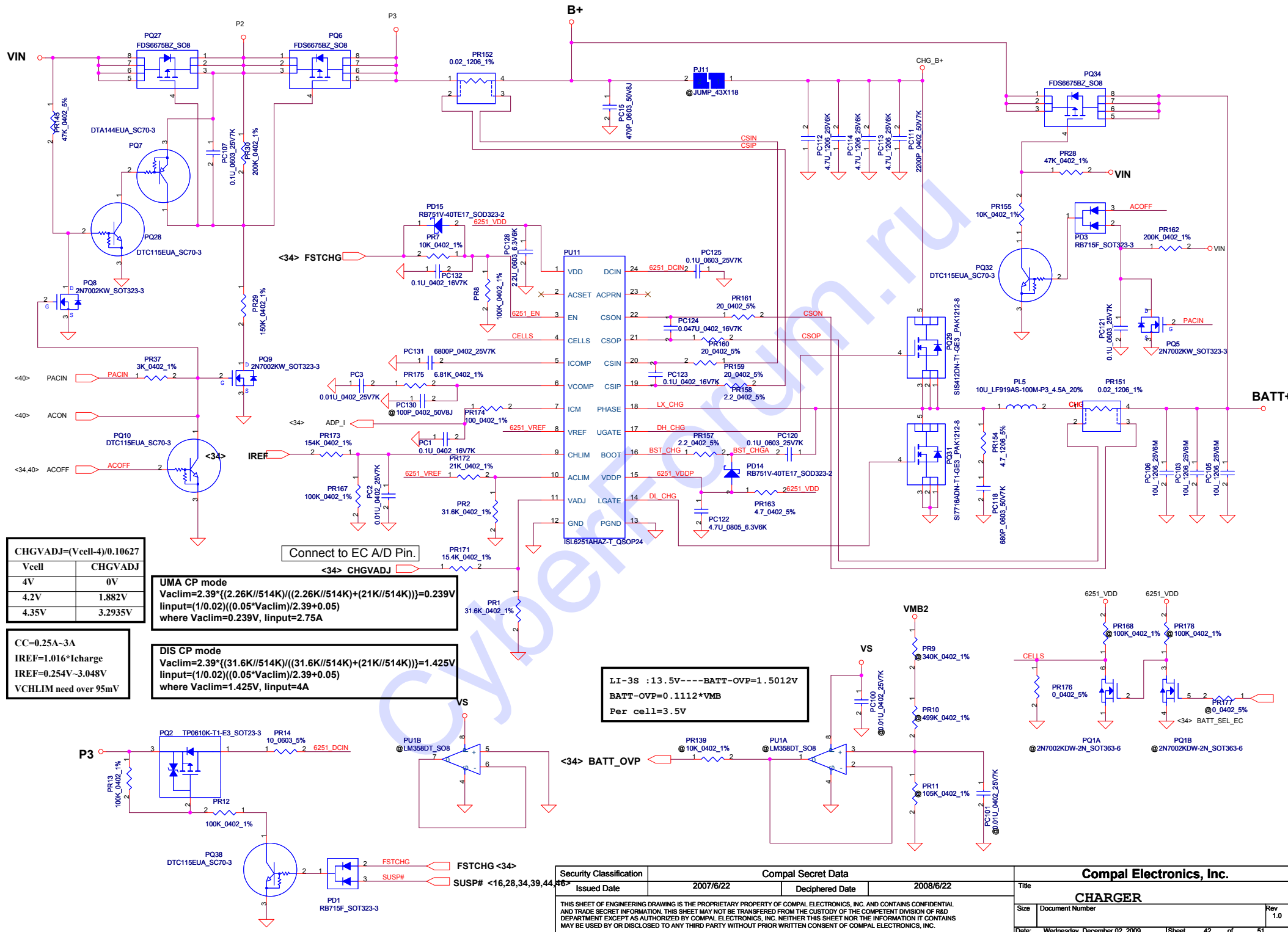
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PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



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CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

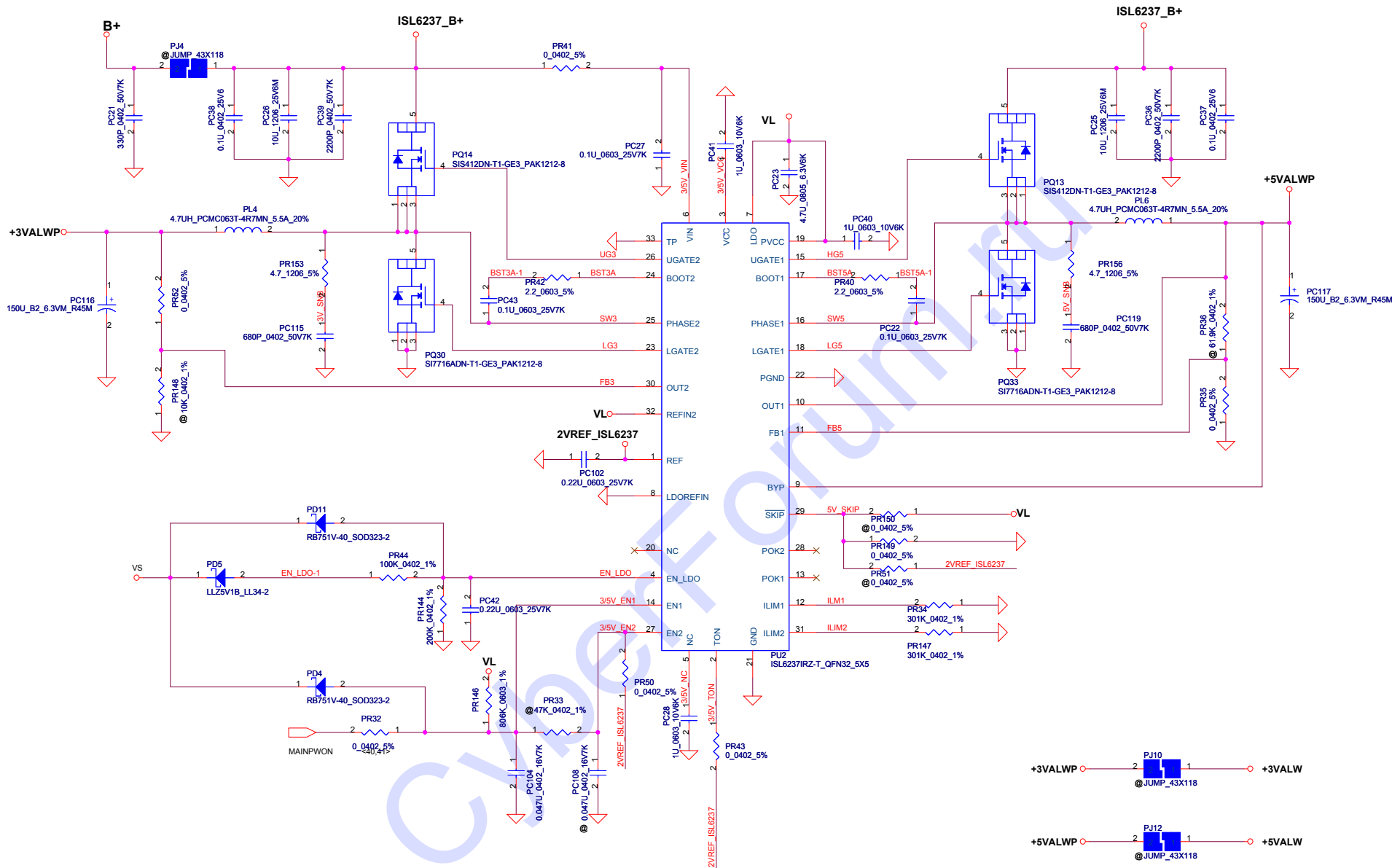
CC=0.25A~3A	
IREF=1.016*Icharge	
IREF=0.254V~3.048V	
VCHLIM need over 95mV	

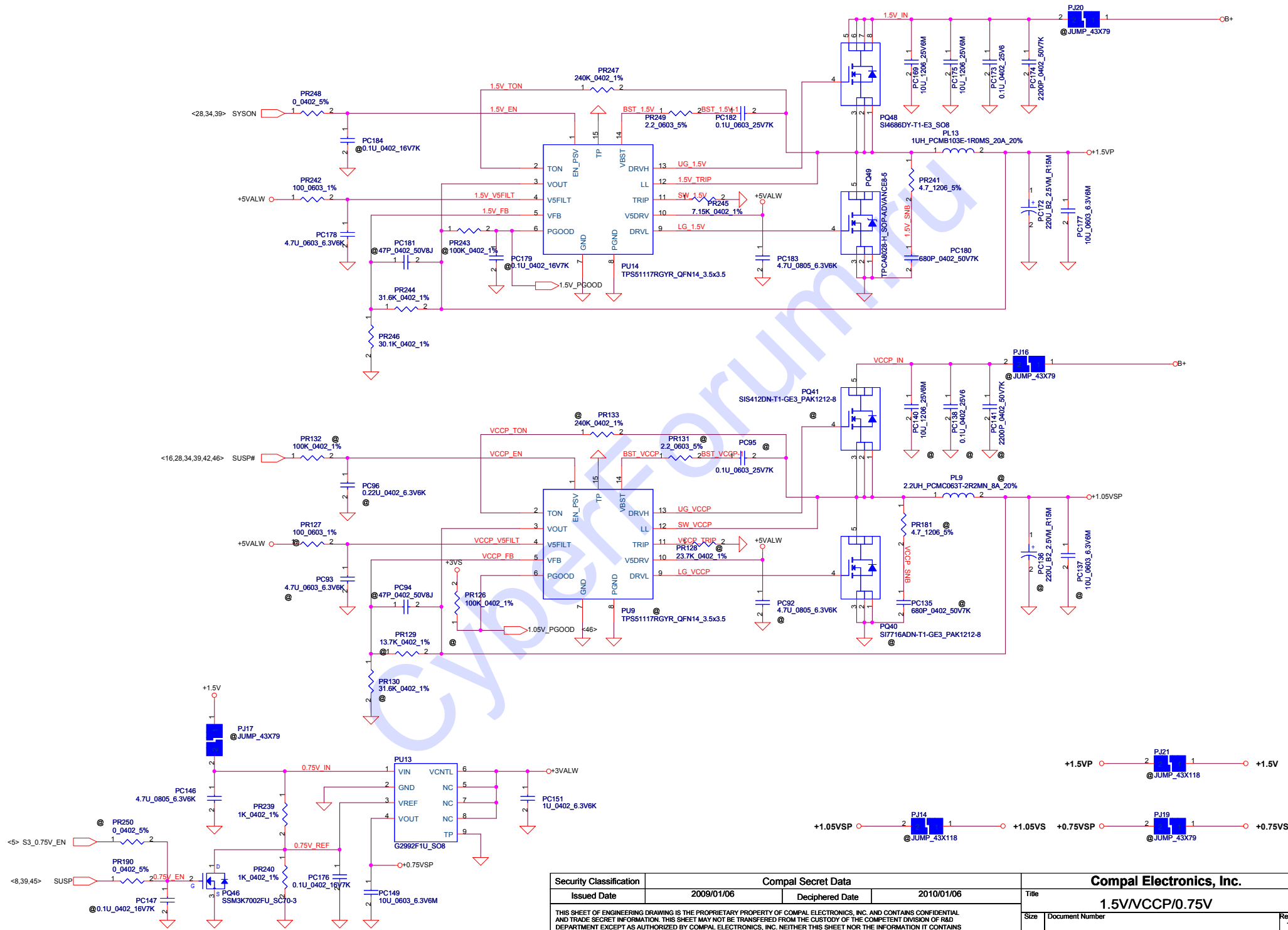
UMA CP mode
 $V_{acim}=2.39*((2.26K//514K)/((2.26K//514K)+(21K//514K)))=0.239V$
 $input=(1/0.02)((0.05*V_{acim})/2.39+0.05)$
where $V_{acim}=0.239V$, $input=2.75A$

DIS CP mode
 $V_{acim}=2.39*((31.6K//514K)/((31.6K//514K)+(21K//514K)))=1.425V$
 $input=(1/0.02)((0.05*V_{acim})/2.39+0.05)$
where $V_{acim}=1.425V$, $input=4A$

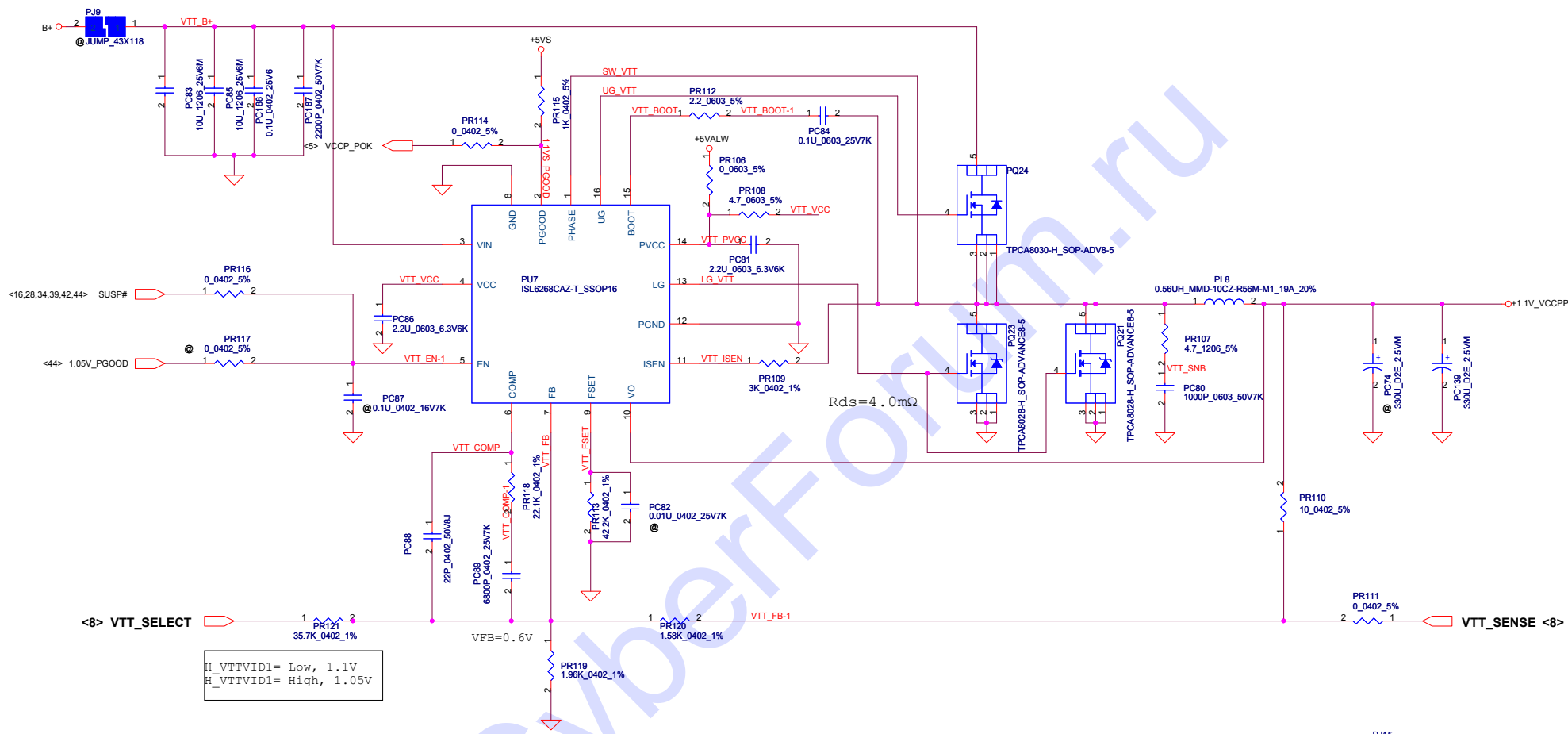
LI-3S : 13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

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								Size	Document Number
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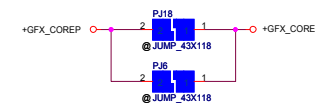




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								Size	Document Number			Rev	
												1.0	
								Date:	Wednesday, December 02, 2009			Sheet	44



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Size		Document Number		Rev	
Custom				1.0	
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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17				20081022	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	EVT TO DVT
1		P15	Add C638~C645	For UMA HDMI	
2		P05	Add test point for BCLK_ITP, BCLK_ITP#, PRDY#	For XDP connector	
3		P32, P28	Change J6 size & unstuff ODD power control components Change J4 size	Disable ODD power control circuit	
4		P17	Stuff C262	For UMA CRT	
5		P34	Change R291, R294 from +3VALW to +3VS		
6		P38	Add R603 pull high to +3VS	For PM_BTN#	
7		P38	Change JP1 from 6 pin to 8 pin , Change JP8 from 14 pin to 12 pin , unstuff R322	For LED color changed Remove CLK_48M_CR	
8		P29, P34	Change EN_WOL to EN_WOL#	For identify clearly	
9		P34	EC pin26-> EC_FAN_PWM , pin75->PCH_TEMP_ALERT , pin34->PROCHOT# , pin66->NOVO#	EC GPIO arrangement	
10		P31	Change JP12 pin define	For EC FAN control	
11		P16	Change U5 pin3, pin5	POWER , GND reversed	
12		P15	Add U28 for ICH_POK & VGATE	Reserved	
13		P12	Unstuff R278, stuff R269 and change U14 to SA00003HQ00	For low power CLK GEN	
14		P13	Change U3 from 2MBytes to 4MBytes	For 4MBytes SPI ROM for PCH	
15		P29	Correct Q17 to P/N:SB000007600	For +3V_LAN power	
16		P16	Add C646 for BUF_PLT_RST#	Reserved for BUF_PLT_RST# overshoot problem	
17		P36	Change U9 from 2MBytes to 256KBytes	For 256KBytes SPI ROM for EC	
18		P03	UMA_HDMI@ , HDMI@ , BT@ , 3G@ , ESATA@ , CMOS@	New BOM structure	
19		P08	Add R608	For PSI# pull down	
20		P37	Delete D18		
21		P16	Unstuff R210, R212	Set Boot BIOS Strap to SPI	
22		P22	Change & stuff R475 to 30K, R51 to 15K Unstuff R474, R50	For N11M-GE1 QS sample	
23		P25	Unstuff R246	Level shift default setting	
24		P39	Change C373 to DIS@	for DIS power sequence	
25		P15, P16, P17	Change R436 from 1K to 10K Change C447 from 0.1u to 1u Delete R514 Unstuff C493, C494 Reserve R609	Check list Rev2.0 update	
27		P34	Add R607	Reserved for KB926 SPI STRAP PIN	
28		P36	Change LED1, LED3, LED4 to white color LED2 to orang\white color and orange connect to +3VALW		
29		P14	Change exp-card from PCIE port 1 to port 5	SW BIOS request	
30		P38	Unstuff SW1		
31		P13, P34	Change X1, X2 footprint		
32		P12	Change C348 to 22p, C349 to 22p	For Crystal matching	
33		P13, P20	Add C647~C650 12p, stuff C370->22p, R331->33	Reserved for RF team	
34		P36	Delete JP6	SPI ROM socket	
35		P37	Change C430, C615 footprint to B2 type		
36		P27, P32, P37	Change Q4, Q24, Q32, Q37 footprint to A03413		

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Title		
HW PIR		
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NO		DATE	PAGE	MODIFICATION LIST	PURPOSE
				EVT TO DVT	
37	P34			Change C320 to 0805 type	
38	P08			Unstuff C268	For CPU VDDQ (DDR3 1.5V rails)
39	P34			Change C252, C258 from 10u to 22u	
40	P31			Change ODD_power_on# from U13 pin28 to pin 76	EC GPIO arrangement
41	P05			Add EC_TACH on U13 pin28 to JP12	
42	P34, P35			Change U20 to EMC1403, add C651	Change thermal sensor solution to EMC1403
43	P34			Add Q42, R610	Reserve for +0.75V enable option
				Add C652, C653, C654	Reserve for NUM_LED#, CAPS_LED# ESD request
				Add R611, R612, R613	For EC_FAN_PWM, EC_TACH
				DVT TO PVT	
				PVT TO Pre-MP	
1	P34			Reseve R614, R615.	EC_ID to identify KB926 D3 or E0
2	P34			Stuff R607	KB926 SPI STRAP PIN
3	P33			Stuff C632~C635	EMI request
4	P16			Stuff C646	For PLT_RST# singnal quality
5	P37			Add R616 100K, change R304 to 100K, C353 to 0.1u	For +3VS_BT power on rising time
6	P37			Changed R304 pin1 from +5VS to +5VALW	For +3VS_BT power on leakage
7	P5			Stuff R283, C338 0.01u	For S3 power reduction
8	P31			Add U29	Colay EMC2103/EMC1403 thermal sensor
				PVT TO Pre-MP	
1	P28			Add R625	For EC to detect debug card
2	P36			Add D29	For WWAN LED
3	P28			Changed R371 to 0 ohm	
4	P08			Changed R140 from 4.7K to 470ohm	For reduce GFX_CORE surge voltage when power off
5	P34			Add new X76	For EC main source(D3) & 2nd source(E0) strapping
6	P38			Add R646	For EC request
7	P16			Changed PM_BTN# pull up from +3VS to +3VALW	
8	P14			Changed C646 from 0.1u to 1u	For PLT_RST# signal quality
9	P17			Stuff Y4, R598, C630, C631	For Integrated Graphics Platforms (25MHz crystal to generate PCH display clocks)
10	P36			Changed R208 from 0 to 1 ohm	For UMA CRT screen wave
11	P14			Changed R359 from 300 to 470 ohm	Reduce LED2 white color brightness
12	P21			Changed C630, C631 from 18p to 27p	For Crystal matching
				Changed L29 from BEAD to 1 ohm	For DIS CRT screen wave

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HW PIR

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